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AB1 PROTOTYPING BOARD USER'S GUIDE

1.0. Summary

The AB1 prototyping board provides a 3 x 3.75" prototyping area (0.1" center through-hole) with access to all MCU I/O signals. Access to I/O signals is provided by a 96-pin, high density connector that mates directly to the expansion connector of C8051F020-TB, C8051F040-TB, C8051F060-TB, and C8051F120-TB target boards. A 128 kB SRAM is installed on the board which can be connected to the MCU's External Memory Interface by installing a single 2-pin jumper (included).

2.0 Features

- 96 pin 3 row connector
- 128 kB SRAM Part number IDT71V124
- SRAM disable jumper J1(open = disabled , closed = enabled)
- Duplicate of connector pins for easy access to signals
- Digital and analog supply and ground rails

3.0 SRAM Details

The IDT71V124SA12PH is a high-speed with 12 nanosecond access and cycle time static SRAM. For more further information on access and cycle times for this SRAM please refer to the IDT71V124 data sheet available at http://www.idt.com/docs/71V124SA_DS_30147.pdf. **To enable the SRAM jumper J1 must be installed and the /CS Chip Select pin must be pulled low.** The SRAM utilizes the External Memory Interface from F02X and later devices, more information on using this interface can be found in Section 16 of the C8051F02x Data Sheet. When enabled the SRAM uses ports 5, 6, and 7 and the upper nibble of port 4. The pin-out is as follows:

Signal Name	SRAM Pin(s)	C8051F02XTB Connection	Description
/WE	12	P4.7	Write Enable
/CS	5	P4.4(J1 closed)	Chip Select
/OE	28	P4.6	Output Enable
VDD	8,24	+3 VD	Digital Power
GND	9,25	GND	Digital Ground
I/O0…I/O7	6,7,10,11,22,23,26,27	P7.0…P7.7	Data Bus
A0…A7	1,2,3,4,13,14,15,16	P6.0…P6.7	Address Bus Low Byte
A8...A15	17,18,19,20,21,29,30,31	P5.0…P5.7	Address Bus High Byte
A16	32	P4.5	Bank Select

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4.0 Hardware Setup

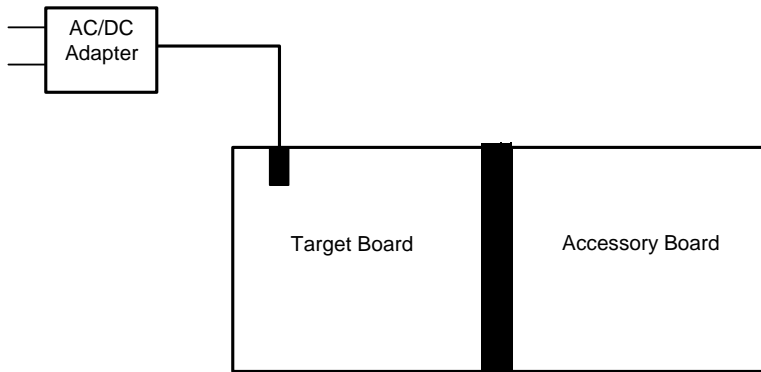A compatible target board is connected to the accessory board as shown in Figure 1.

Figure 1. Hardware Setup

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Datasheet of AB1 - PROTO BOARD W/SRAM FOR C8051
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Notes:

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