



# C8051F330-GDI

## 1. Ordering Information

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)*	RAM (Bytes)	SMBus/I <sup>2</sup> C	UART	Enhanced SPI	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200 ksps ADC	Internal Voltage Reference	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Wafer Thickness
C8051F330-G1DI	25	8	768	1	1	1	4	✓	17	✓	✓	✓	1	✓	28.5433 mil / 725 μm (No backgrind)
C8051F330-GDI	25	8	768	1	1	1	4	✓	17	✓	✓	✓	1	✓	12 mil (backgrind)

**\*Note:** 512 bytes reserved for factory use.

## 2. Pin Definitions

**Table 2.1. Pin Definitions for the C8051F330-GDI \***

Name	Physical Pad Number	Type	Description
V <sub>DD</sub>	4,5		Power Supply Voltage.
GND	2,3		Ground.
$\overline{\text{RST}}$	6	D I/O	Device Reset. Open-drain output of internal POR or V <sub>DD</sub> monitor. An external source can initiate a system reset by driving this pin low for at least 10 $\mu\text{s}$ .
C2CK		D I/O	Clock signal for the C2 Debug Interface.
P2.0/	7	D I/O	Port 2.0.
C2D		D I/O	Bi-directional data signal for the C2 Debug Interface.
P0.0/	1	D I/O or A In	Port 0.0.
VREF		A In	External VREF input.
P0.1	26	D I/O or A In	Port 0.1.
IDA0		AOut	IDA0 Output.
P0.2/	25	D I/O or A In	Port 0.2.
XTAL1		A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/	24	D I/O or A In	Port 0.3.
XTAL2		A I/O or D In	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	23	D I/O or A In	Port 0.4.
P0.5	22	D I/O or A In	Port 0.5.

**\*Note:** For a complete description of the functionality of all pins, refer to the C8051F330/1/2/3/4/5 technical data sheet.

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Table 2.1. Pin Definitions for the C8051F330-GDI (Continued)\*

Name	Physical Pad Number	Type	Description
P0.6/ CNVSTR	21	D I/O or A In  D In	Port 0.6.  ADC0 External Convert Start or IDA0 Update Source Input.
P0.7	20	D I/O or A In	Port 0.7.
P1.0	18	D I/O or A In	Port 1.0.
P1.1	16	D I/O or A In	Port 1.1.
P1.2	15	D I/O or A In	Port 1.2.
P1.3	14	D I/O or A In	Port 1.3.
P1.4	11	D I/O or A In	Port 1.4.
P1.5	10	D I/O or A In	Port 1.5.
P1.6	9	D I/O or A In	Port 1.6.
P1.7	8	D I/O or A In	Port 1.7.

**\*Note:** For a complete description of the functionality of all pins, refer to the C8051F330/1/2/3/4/5 technical data sheet.

## 3. Bonding Instructions

Table 3.1. C8051F330-GDI Pad Connections

Physical Pad Number	Package Pin Number (20-QFN)	Package Pin Name	Physical Pad X (μm)	Physical Pad Y (μm)
1	P0.0	1	-802.7	964.7
2	GND	2	-964.7	-61.2
3	GND	2	-964.7	-173.2
4	VDD	3	-964.7	-284.1
5	VDD	3	-964.7	-396.1
6	/RST/C2CK	4	-964.7	-587.7
7	P2.0/C2D	5	-964.7	-797.7
8	P1.7	6	-797.7	-964.7
9	P1.6	7	-627.7	-964.7
10	P1.5	8	-447.7	-964.7
11	P1.4	9	240.7	-964.7
12	Reserved*	—	396.7	-964.7
13	Reserved*	—	471.7	-964.7
14	P1.3	10	627.7	-964.7
15	P1.2	11	797.7	-964.7
16	P1.1	12	964.7	-797.7
17	Reserved*	—	964.7	70.05
18	P1.0	13	964.7	201.05
19	Reserved*	—	964.7	337.05
20	P0.7	14	964.7	627.7
21	P0.6	15	964.7	797.7
22	P0.5	16	797.7	964.7
23	P0.4	17	627.7	964.7
24	P0.3	18	447.7	964.7
25	P0.2	19	-79.9	964.7
26	P0.1	20	-622.7	964.7

**\*Note:** Pins marked "Reserved" should not be connected.

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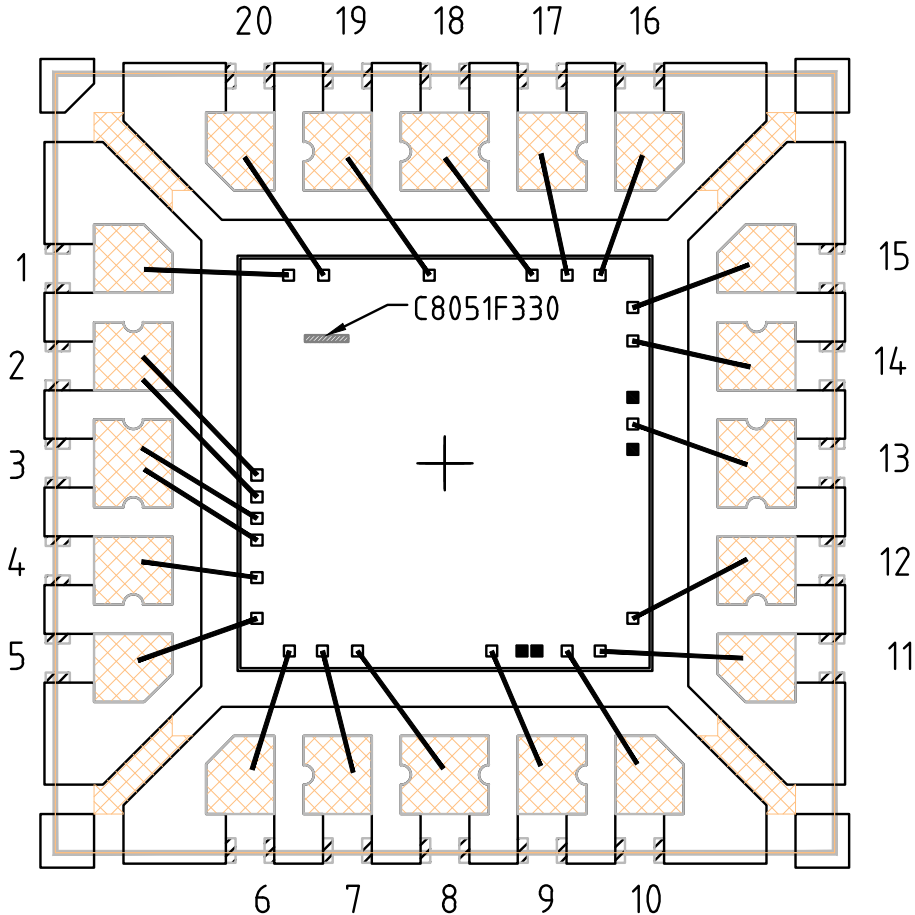


Figure 3.1. Example Die Bonding (QFN-20)

**Table 3.2. Wafer and Die Information**

<b>Wafer ID</b>	C8051F330
<b>Wafer Dimensions</b>	8 in
<b>Die Dimensions</b>	2.13 mm x 2.13 mm
<b>Wafer Thickness (no backgrind)</b>	28.54 mil $\pm$ 1 mil (725 $\mu$ m)
<b>Wafer Thickness (with backgrind)</b>	12 mil $\pm$ 1 mil
<b>Wafer Identification</b>	Notch
<b>Scribe Line Width</b>	80 $\mu$ m
<b>Die Per Wafer*</b>	Contact Sales for info
<b>Passivation</b>	Standard
<b>Wafer Packaging Detail</b>	Wafer Jar
<b>Bond Pad Dimensions</b>	60 $\mu$ m x 60 $\mu$ m
<b>Maximum Processing Temperature</b>	250 °C
<b>Electronic Die Map Format</b>	.txt
<b>Bond Pad Pitch Minimum</b>	75 $\mu$ m
<b>*Note:</b> This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).	

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## 4. Wafer Storage Guidelines

It is necessary to conform to appropriate wafer storage practices to avoid product degradation or contamination.

- Wafers may be stored for up to 18 months in the original packaging supplied by Silicon Labs.
- Wafers must be stored at a temperature of 18–24 °C.
- Wafers must be stored in a humidity-controlled environment with a relative humidity of <30%.
- Wafers should be stored in a clean, dry, inert atmosphere (e.g. nitrogen or clean, dry air).



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## 5. Failure Analysis (FA) Guidelines

Certain conditions must be met for Silicon Laboratories to perform Failure Analysis on devices sold in wafer form.

- In order to conduct failure analysis on a device in a customer-provided package, Silicon Laboratories must be provided with die assembled in an industry standard package that is pin compatible with existing packages Silicon Laboratories offers for the device. Initial response time for FA requests that meet this requirements will follow the standard FA guidelines for packaged parts.
- If retest of the entire wafer is requested, Silicon Laboratories must be provided with the whole wafer. Silicon Laboratories cannot retest any wafers that have been sawed, diced, backgrind or are on tape. Initial response time for FA requests that meet this requirements will be 3 weeks.

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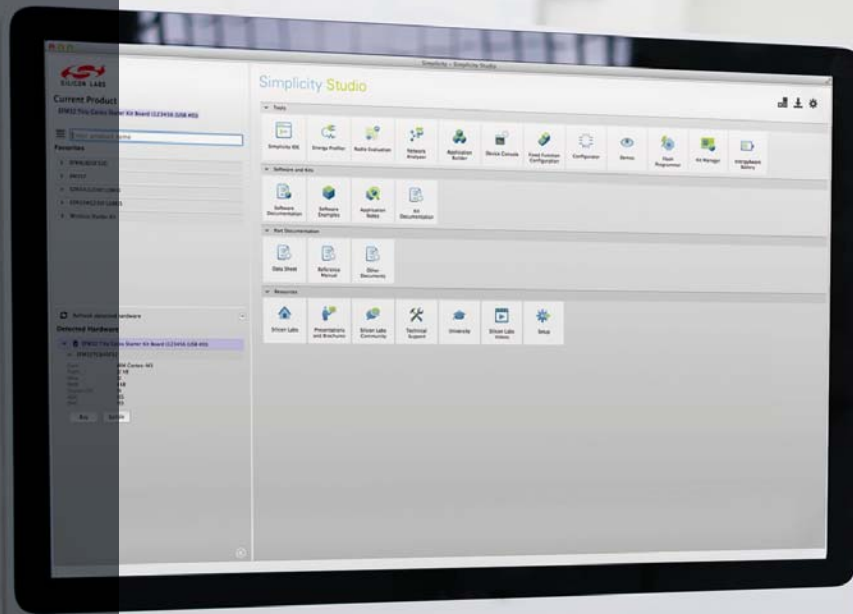
## DOCUMENT CHANGE LIST

### Revision 1.0 to Revision 1.1

- Changed Wafer Packaging Detail to “Wafer Jar” in Table 3.2 on page 7.

### Revision 1.1 to Revision 1.2

- Updated Table 1.1, “Product Selection Guide,” on page 2.
- Updated Table 3.2, “Wafer and Die Information,” on page 7.
- Added “5. Failure Analysis (FA) Guidelines” on page 9.



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