

## DUAL 1:3 LOW-JITTER ANY-FORMAT BUFFER/LEVEL TRANSLATOR

### Features

- Two independent banks of 3 differential or 6 LVCMOS outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: dc to 725 MHz
- Any-format input with pin selectable output formats: LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS
- Synchronous output enable
- Output clock division: /1, /2, /4
- Low output-output skew: 25 ps
- Loss of signal (LOS) monitors for loss of input clock
- Independent  $V_{DD}$  and  $V_{DDO}$  : 1.8/2.5/3.3 V
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 32-QFN (5 mm x 5 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: -40 to +85 °C

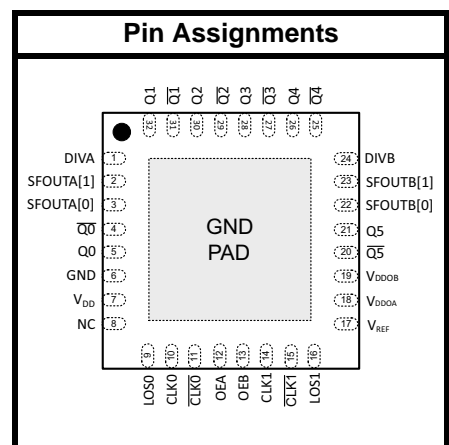
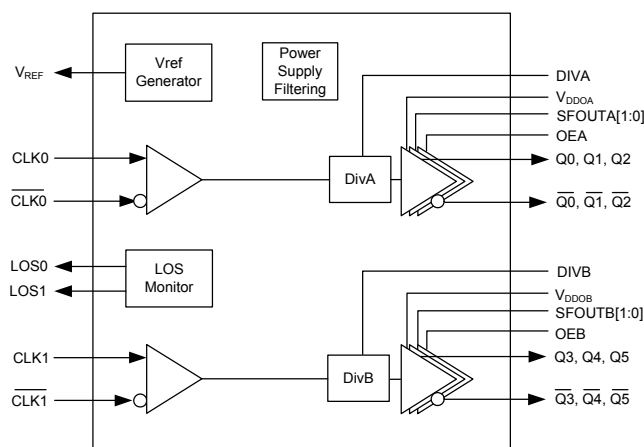
### Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage/Servers
- Telecom
- Industrial
- SyncE, 1588
- Backplane clock distribution

### Description

The Si53308 is an ultra low jitter dual 1:3 any-format buffer with pin-selectable output clock signal format and divider selection. The Si53308 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from dc to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53308 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

### Functional Block Diagram



Patents pending



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**TABLE OF CONTENTS**


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<b><u>Section</u></b>	<b><u>Page</u></b>
<b>1. Electrical Specifications</b> .....	<b>4</b>
<b>2. Functional Description</b> .....	<b>12</b>
2.1. Universal, Any-Format Input .....	13
2.2. Input Bias Resistors .....	15
2.3. Universal, Any-Format Output Buffer .....	15
2.4. Synchronous Output Enable .....	16
2.5. Flexible Output Divider .....	16
2.6. Output Enable Logic .....	16
2.7. Loss of Signal (LOS) Indicator .....	17
2.8. Power Supply ( $V_{DD}$ and $V_{DDOX}$ ) .....	17
2.9. Output Clock Termination Options .....	18
2.10. AC Timing Waveforms .....	21
2.11. Typical Phase Noise Performance .....	22
2.12. Input Noise Isolation .....	25
2.13. Power Supply Noise Rejection .....	25
<b>3. Pin Description: 32-Pin QFN</b> .....	<b>26</b>
<b>4. Ordering Guide</b> .....	<b>29</b>
<b>5. Package Outline</b> .....	<b>30</b>
5.1. 5x5 mm 32-QFN Package Diagram .....	30
<b>6. PCB Land Pattern</b> .....	<b>31</b>
6.1. 5x5 mm 32-QFN Package Land Pattern .....	31
<b>7. Top Marking</b> .....	<b>32</b>
7.1. Si53308 Top Marking .....	32
7.2. Top Marking Explanation .....	32
<b>Document Change List</b> .....	<b>33</b>

## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	$T_A$		-40	—	85	°C
Supply Voltage Range*	$V_{DD}$	LVDS, CML	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		LVPECL, low power LVPECL, LVC MOS	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		HCSL	2.97	3.3	3.63	V
Output Buffer Supply Voltage*	$V_{DDOX}$	LVDS, CML, LVC MOS	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		LVPECL, low power LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		HCSL	2.97	3.3	3.63	V

**\*Note:** Core supply  $V_{DD}$  and output buffer supplies  $V_{DDOX}$  are independent. LVC MOS clock input is not supported for  $V_{DD} = 1.8V$  but is supported for LVC MOS clock output for  $V_{DDOX} = 1.8V$ . LVC MOS outputs at 1.5V and 1.2V can be supported via a simple resistor divider network. See “2.9.1. LVC MOS Output Termination To Support 1.5 V and 1.2 V”

**Table 2. Input Clock Specifications**

( $V_{DD}=1.8 V \pm 5\%$ ,  $2.5 V \pm 5\%$ , or  $3.3 V \pm 10\%$ ,  $T_A=-40$  to  $85$  °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	$V_{CM}$		0.05	—	—	V
Differential Input Swing (peak-to-peak)	$V_{IN}$		0.2	—	2.2	V
LVC MOS Input High Voltage	$V_{IH}$	$V_{DD} = 2.5 V \pm 5\%$ , $3.3 V \pm 10\%$	$V_{DD} \times 0.7$	—	—	V
LVC MOS Input Low Voltage	$V_{IL}$	$V_{DD} = 2.5 V \pm 5\%$ , $3.3 V \pm 10\%$	—	—	$V_{DD} \times 0.3$	V
Input Capacitance	$C_{IN}$	CLK0 and CLK1 pins with respect to GND	—	5	—	pF

**Table 3. DC Common Characteristics** $(V_{DD} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40 \text{ to } 85\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	$I_{DD}$		—	65	100	mA
Output Buffer Supply Current (Per Clock Output) @100 MHz (diff) @200 MHz (CMOS)	$I_{DDOX}$	LVPECL (3.3 V)	—	35	—	mA
		Low Power LVPECL (3.3 V)*	—	35	—	mA
		LVDS (3.3 V)	—	20	—	mA
		CML (3.3 V)	—	35	—	mA
		HCSL, 100 MHz, 2 pF load (3.3 V)	—	35	—	mA
		CMOS (1.8 V, SFOUT = Open/0), per output, $C_L = 5\text{ pF}$ , 200 MHz	—	5	—	mA
		CMOS (2.5 V, SFOUT = Open/0), per output, $C_L = 5\text{ pF}$ , 200 MHz	—	8	—	mA
CMOS (3.3 V, SFOUT = 0/1), per output, $C_L = 5\text{ pF}$ , 200 MHz	—	15	—	mA		
Voltage Reference	$V_{REF}$	$V_{REF}$ pin $-500\text{ }\mu\text{A} < I_{REF} < 500\text{ }\mu\text{A}$	—	VDD/2	—	V
Input High Voltage	$V_{IH}$	SFOUTx, DIVx CLK_SEL, OEx	0.8 x VDD	—	—	V
Input Mid Voltage	$V_{IM}$	SFOUTx, DIVx 3-level input pins	0.45 x VDD	0.5 x VDD	0.55 x VDD	V
Input Low Voltage	$V_{IL}$	SFOUTx, DIVx CLK_SEL, OEx	—	—	0.2 x VDD	V
Output Voltage High (LOSx)	$V_{OH}$	$I_{DD} = -1\text{ mA}$	0.8xVDD	—	—	V
Output Voltage Low (LOSx)	$V_{OL}$	$I_{DD} = 1\text{ mA}$	—	—	0.2xVDD	V
Internal Pull-down Resistor	$R_{DOWN}$	CLK_SEL, DIVx, SFOUTx	—	25	—	k $\Omega$
Internal Pull-up Resistor	$R_{UP}$	OEx, DIVx, SFOUTx	—	25	—	k $\Omega$

\*Note: Low-power LVPECL mode supports an output termination scheme that will reduce overall system power.

**Table 4. Output Characteristics (LVPECL)**

( $V_{DDOX} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	$V_{COM}$		$V_{DDOX} - 1.595$	—	$V_{DDOX} - 1.245$	V
Single-Ended Output Swing*	$V_{SE}$		0.55	0.80	1.050	V

\*Note: Unused outputs can be left floating. Do not short unused outputs to ground.

**Table 5. Output Characteristics (Low Power LVPECL)**

( $V_{DDOX} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	$V_{COM}$	$R_L = 100\ \Omega$ across $Q_n$ and $\overline{Q_n}$	$V_{DDOX} - 1.895$		$V_{DDOX} - 1.275$	V
Single-Ended Output Swing	$V_{SE}$	$R_L = 100\ \Omega$ across $Q_n$ and $\overline{Q_n}$	0.25	0.60	0.85	V

**Table 6. Output Characteristics—CML**

( $V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	$V_{SE}$	Terminated as shown in Figure 8 (CML termination).	300	400	550	mV

**Table 7. Output Characteristics—LVDS**

( $V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	$V_{SE}$	$R_L = 100\ \Omega$ across $Q_N$ and $\overline{Q_N}$	247	—	490	mV
Output Common Mode Voltage ( $V_{DDO} = 2.5\text{ V}$ or $3.3\text{ V}$ )	$V_{COM1}$	$V_{DDOX} = 2.38$ to $2.63\text{ V}$ , $2.97$ to $3.63\text{ V}$ , $R_L = 100\ \Omega$ across $Q_N$ and $\overline{Q_N}$	1.10	1.25	1.35	V
Output Common Mode Voltage ( $V_{DDO} = 1.8\text{ V}$ )	$V_{COM2}$	$V_{DDOX} = 1.71$ to $1.89\text{ V}$ , $R_L = 100\ \Omega$ across $Q_N$ and $\overline{Q_N}$	0.85	0.97	1.25	V

**Table 8. Output Characteristics—LVCMOS** $(V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High*	$V_{OH}$		$0.75 \times V_{DDOX}$	—	—	V
Output Voltage Low*	$V_{OL}$		—	—	$0.25 \times V_{DDOX}$	V

\*Note:  $I_{OH}$  and  $I_{OL}$  per the Output Signal Format Table for specific  $V_{DDOX}$  and SFOUTX settings. All LVCMOS outputs are in-phase.

**Table 9. Output Characteristics—HCSL** $(V_{DDOX} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	$V_{OH}$	$R_L = 50\ \Omega$ to GND	550	700	900	mV
Output Voltage Low	$V_{OL}$	$R_L = 50\ \Omega$ to GND	-150	0	150	mV
Single-Ended Output Swing	$V_{SE}$	$R_L = 50\ \Omega$ to GND	550	700	850	mV
Crossing Voltage	$V_C$	$R_L = 50\ \Omega$ to GND	250	350	550	mV

**Table 10. AC Characteristics** $(V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )<sup>1</sup>

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LOSx Clear Time	$T_{LOSCLR}$	$1\text{ MHz} \leq F < 100\text{ MHz}$	—	$T_{per}+15$	—	ns
		$F > 100\text{ MHz}$	—	25	—	ns
LOSx Activation Time	$T_{LOSACT}$	$1\text{ MHz} \leq F \leq 725\text{ MHz}$	—	15	—	$\mu\text{s}$
Frequency	F	LVPECL, low power LVPECL, LVDS, CML, HCSL	dc	—	725	MHz
		LVCMOS	dc	—	200	MHz
Duty Cycle Note: 50% input duty cycle.	$D_C$	200 MHz, 20/80% $T_R/T_F < 10\%$ of period (LVCMOS) (12 mA drive)	40	50	60	%
		20/80% $T_R/T_F < 10\%$ of period (Differential)	48	50	52	%

**Notes:**

1. See the Output Characteristics tables for operating voltage specifications for various outputs formats.
2. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
3. HCSL measurements were made with receiver termination. See Figure 8 on page 19.
4. Output to Output skew specified for outputs with an identical configuration.
5. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
6. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to  $V_{DDOX}$  ( $3.3\text{ V} = 100\text{ mV}_{PP}$ ) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

**Table 10. AC Characteristics (Continued)**

( $V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ )<sup>1</sup>

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Input Clock Slew Rate <sup>2</sup>	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	$T_R/T_F$	LVDS, 20/80%	—	—	325	ps
		LVPECL, 20/80% $V_{DDOX} = 2.5\text{ V}, 3.3\text{ V}$	—	—	350	ps
		HCSL <sup>3</sup> , 20/80% $V_{DDOX} = 3.3\text{ V}$	—	—	280	ps
		CML, 20/80%	—	—	350	ps
		Low-Power LVPECL, 20/80% $V_{DDOX} = 2.5\text{ V}, 3.3\text{ V}$	—	—	325	ps
		LVC MOS 200 MHz, 20/80%, 2 pF load	—	—	750	ps
Minimum Input Pulse Width	$T_W$		500	—	—	ps
Propagation Delay	$T_{PLH}, T_{PHL}$	LVC MOS (12mA drive with no load)	1250	2000	2750	ps
		LVPECL, LVDS	600	800	1000	ps
Output Enable Time	$T_{EN}$	F = 1 MHz	—	2500	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	5	—	ns
Output Disable Time	$T_{DIS}$	F = 1 MHz	—	2000	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	5	—	ns
Output to Output Skew <sup>4</sup>	$T_{SK}$	LVC MOS (12 mA drive to no load)	—	50	120	ps
		LVPECL $V_{DDOX} = 2.5\text{ V}, 3.3\text{ V}$	—	35	70	ps
		LVDS	—	35	70	ps
Part to Part Skew <sup>5</sup>	$T_{PS}$	Differential	—	—	150	ps

**Notes:**

1. See the Output Characteristics tables for operating voltage specifications for various outputs formats.
2. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
3. HCSL measurements were made with receiver termination. See Figure 8 on page 19.
4. Output to Output skew specified for outputs with an identical configuration.
5. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
6. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to  $V_{DDOX}$  ( $3.3\text{ V} = 100\text{ mV}_{PP}$ ) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.



**Table 10. AC Characteristics (Continued)** $(V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40\text{ to } 85\text{ }^\circ\text{C})^1$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Noise Rejection <sup>6</sup>	PSRR	10 kHz sinusoidal noise	—	-65	—	dBc
		100 kHz sinusoidal noise	—	-63	—	dBc
		500 kHz sinusoidal noise	—	-60	—	dBc
		1 MHz sinusoidal noise	—	-55	—	dBc

**Notes:**

1. See the Output Characteristics tables for operating voltage specifications for various outputs formats.
2. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
3. HCSL measurements were made with receiver termination. See Figure 8 on page 19.
4. Output to Output skew specified for outputs with an identical configuration.
5. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
6. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to  $V_{DDOX}$  ( $3.3\text{ V} = 100\text{ mV}_{PP}$ ) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

**Table 11. Additive Jitter, Differential Clock Input**

$V_{DD}$	Input <sup>1,2</sup>				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz) <sup>3</sup>	
	Freq (MHz)	Clock Format	Amplitude $V_{IN}$ (Single-Ended, Peak-to-Peak)	Differential 20%-80% Slew Rate (V/ns)		Clock Format	Typ
3.3	725	Differential	0.15	0.637	LVPECL	45	65
3.3	725	Differential	0.15	0.637	LVDS	50	65
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
3.3	156.25	Differential	0.5	0.458	LVDS	150	200
2.5	725	Differential	0.15	0.637	LVPECL	45	65
2.5	725	Differential	0.15	0.637	LVDS	50	65
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185
2.5	156.25	Differential	0.5	0.458	LVDS	145	195

**Notes:**

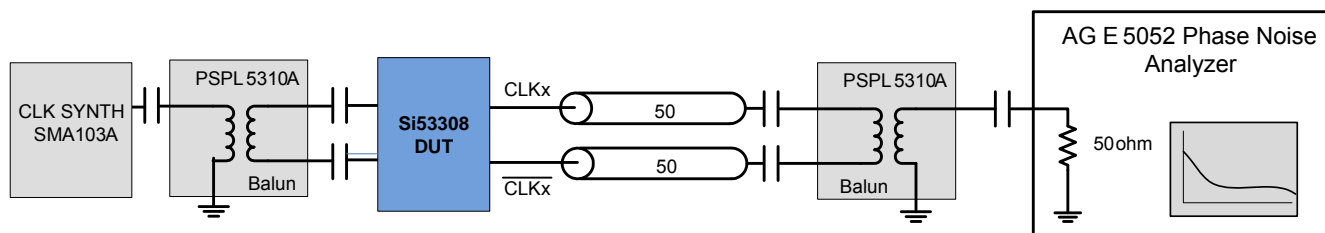
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

**Table 12. Additive Jitter, Single-Ended Clock Input**

V <sub>DD</sub>	Input <sup>1,2</sup>				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz) <sup>3</sup>	
	Freq (MHz)	Clock Format	Amplitude V <sub>IN</sub> (single-ended, peak to peak)	SE 20%-80% Slew Rate (V/ns)		Clock Format	Typ
3.3	200	Single-ended	1.70	1	LVC MOS <sup>4</sup>	120	160
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
3.3	156.25	Single-ended	2.18	1	LVDS	150	200
3.3	156.25	Single-ended	2.18	1	LVC MOS <sup>4</sup>	130	180
2.5	200	Single-ended	1.70	1	LVC MOS <sup>5</sup>	120	160
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185
2.5	156.25	Single-ended	2.18	1	LVDS	145	195
2.5	156.25	Single-ended	2.18	1	LVC MOS <sup>5</sup>	140	180

**Notes:**

1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1. LVC MOS jitter is measured single-ended.
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11).
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11).



**Figure 1. Differential Measurement Method Using a Balun**

Table 13. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Still air	49.6	°C/W
Thermal Resistance, Junction to Case	$\theta_{JC}$	Still air	32.3	°C/W

Table 14. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	$T_S$		-55	—	150	°C
Supply Voltage	$V_{DD}$		-0.5	—	3.8	V
Input Voltage	$V_{IN}$		-0.5	—	$V_{DD} + 0.3$	V
Output Voltage	$V_{OUT}$		—	—	$V_{DD} + 0.3$	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 k $\Omega$	—	—	2000	V
ESD Sensitivity	CDM		—	—	500	V
Peak Soldering Reflow Temperature	$T_{PEAK}$	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	$T_J$		—	—	125	°C

**Note:** Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 2. Functional Description

The Si53308 is a low-jitter, low-skew, dual 1:3 differential output buffer. The device has a universal input that accepts most common differential or LVCMOS input signals. Each output bank features control pins to select signal format, output enable, output divider setting and LVCMOS drive strength.

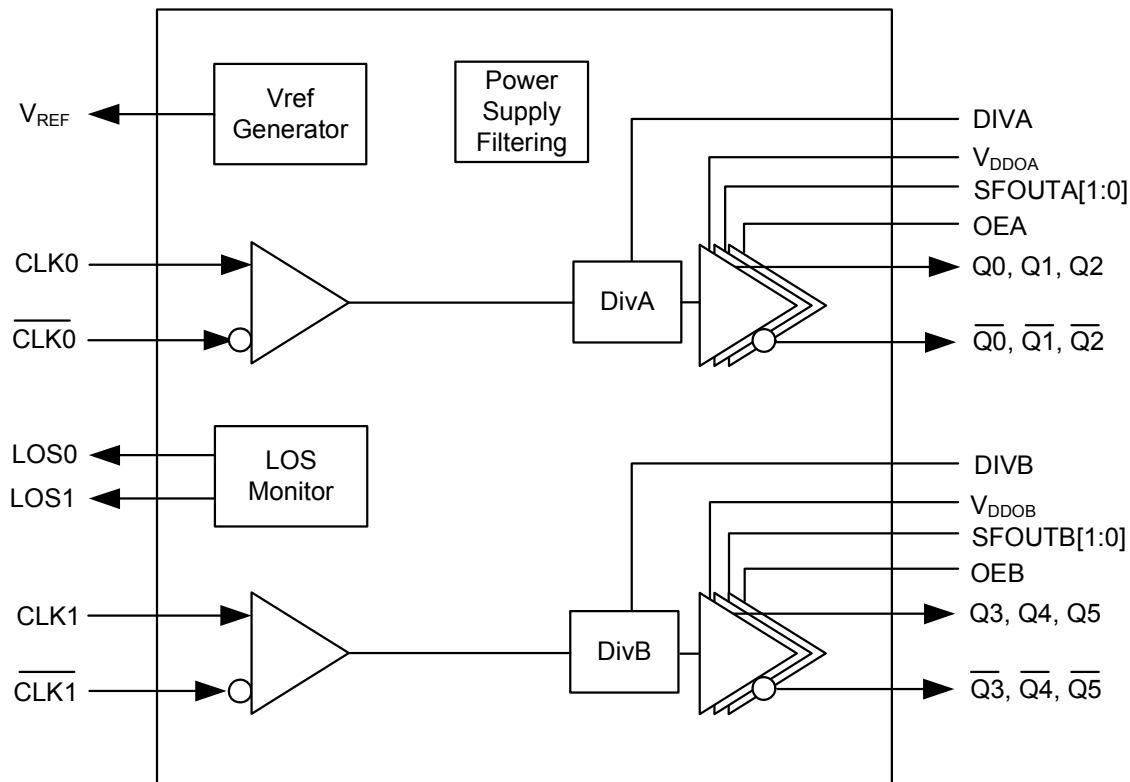


Figure 2. Functional Block Diagram

## 2.1. Universal, Any-Format Input

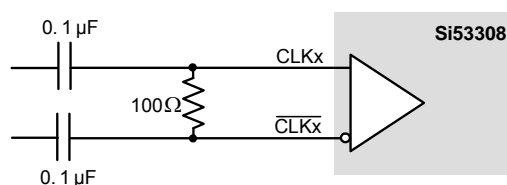
The Si53308 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 15 and 16 summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended as low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

**Table 15. LVPECL, LVCMOS, and LVDS**

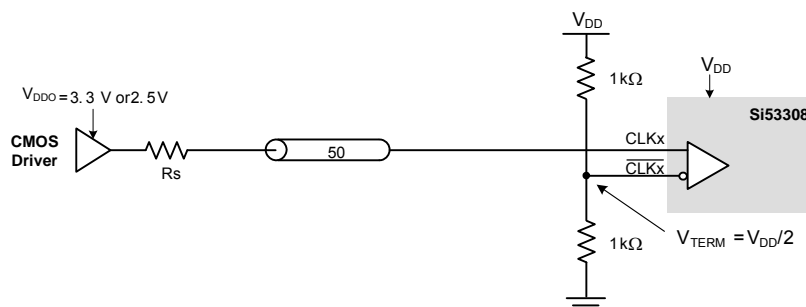
	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	N/A	N/A	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

**Table 16. HCSL and CML**

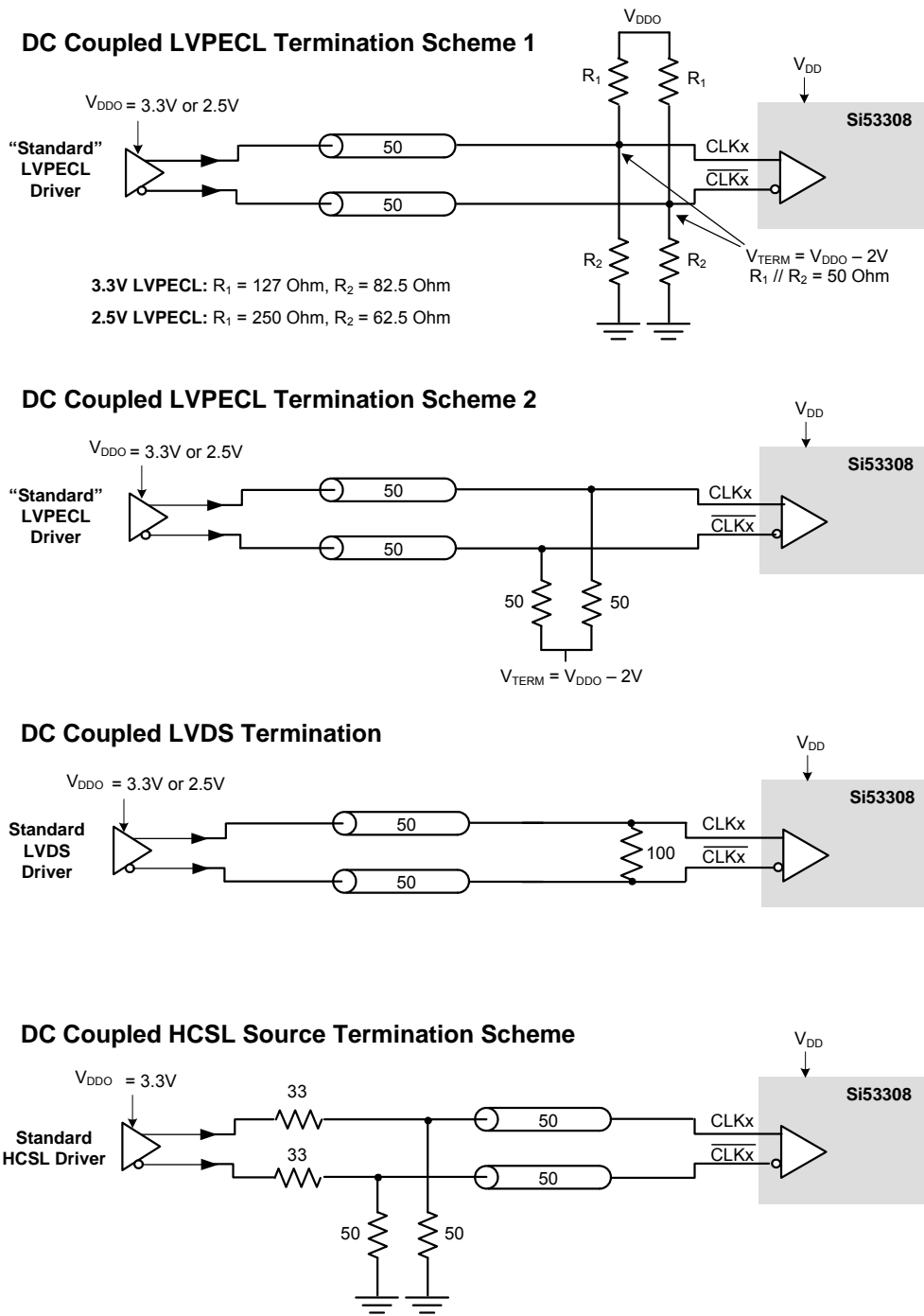
	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	Yes	No
2.5/3.3 V	Yes	Yes	Yes	No



**Figure 3. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination**



**Figure 4. LVCMOS DC-Coupled Input Termination**

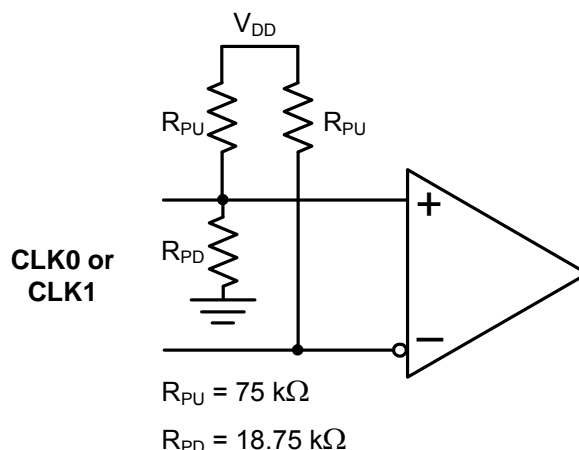


Note: 33 Ohm series termination is optional depending on the location of the receiver.

**Figure 5. Differential DC-Coupled Input Terminations**

## 2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V<sub>DD</sub>. The inverting input is biased with a 75 kΩ pullup to V<sub>DD</sub>.



**Figure 6. Input Bias Resistors**

## 2.3. Universal, Any-Format Output Buffer

The Si53308 has highly flexible output drivers that support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTX[1] and SFOUTX[0] are 3-level inputs that can be pin-strapped to select the Bank A or Bank B clock signal formats. This feature enables the device to be used for format translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each V<sub>DDOX</sub> setting.

**Table 17. Output Signal Format Selection**

SFOUTX[1]	SFOUTX[0]	V <sub>DDOX</sub> = 3.3 V	V <sub>DDOX</sub> = 2.5 V	V <sub>DDOX</sub> = 1.8 V
Open*	Open*	LVPECL	LVPECL	N/A
0	0	LVDS	LVDS	LVDS
0	1	LVCMOS, 24 mA drive	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive
1	0	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive
1	1	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive	LVCMOS, 6 mA drive
Open*	0	LVCMOS, 6 mA drive	LVCMOS, 4 mA drive	LVCMOS, 2 mA drive
Open*	1	LVPECL low power	LVPECL low power	N/A
0	Open*	CML	CML	CML
1	Open*	HCSL	N/A	N/A

**\*Note:** SFOUTX are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin is internally biased to V<sub>DD</sub>/2.

## 2.4. Synchronous Output Enable

The Si53308 features a synchronous output enable (disable) feature for input frequencies between 1 MHz and 725 MHz. Output enable is sampled and synchronized on the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.

When OE is low, Q is held low and  $\bar{Q}$  is held high for differential output formats. For LVCMOS output format options, both Q and  $\bar{Q}$  are held low when OE is set low. The device outputs are enabled when the output enable pin is unconnected. See Table 10 for output enable and output disable times.

## 2.5. Flexible Output Divider

The Si53308 provides optional clock division in addition to clock distribution. The divider setting for each bank of output clocks is selected via 3-level control pins as shown in the table below. Leaving the DIVx pins open will force a divider value of 1 which is the default mode of operation.

**Note:** When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.

**Table 18. Post Divider Selection**

DIVx	Divider Value
Open*	÷1 (default)
0	÷2
1	÷4

**\*Note:** DIVx are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin is internally biased to VDD/2.

## 2.6. Output Enable Logic

Each 1:3 output has an independent clock input (CLK0/CLK1) and an output enable pin. Table 19 summarizes the input and output clock based upon the state of the input clock and the OE pin.

**Table 19. Input Clock and Output Enable Logic**

CLK	OE <sup>1</sup>	Q <sup>2</sup>
L	H	L
H	H	H
X	L	L <sup>3</sup>

**Notes:**

- Output enable active high.
- On the next negative transition of CLK0 or CLK1.
- Single-end: Q = low,  $\bar{Q}$  = low.  
Differential: Q = low,  $\bar{Q}$  = high.



## 2.7. Loss of Signal (LOS) Indicator

The LOS0 and LOS1 indicators are used to check for the presence of input clocks CLK0 and CLK1, respectively, for input frequencies between 1 MHz and 725 MHz. The LOS0 and LOS1 pins are checked prior to selecting that clock input or are polled to check for the presence of the currently selected input clock. In the event that an input clock is not present, the associated LOSx pin will assume a logic high (LOSx = 1) state. When a clock is present at the associated input clock pin, the LOSx pin will assume a logic low (LOSx = 0) state.

**Note:** LOS has a lower frequency specification (1 MHz).

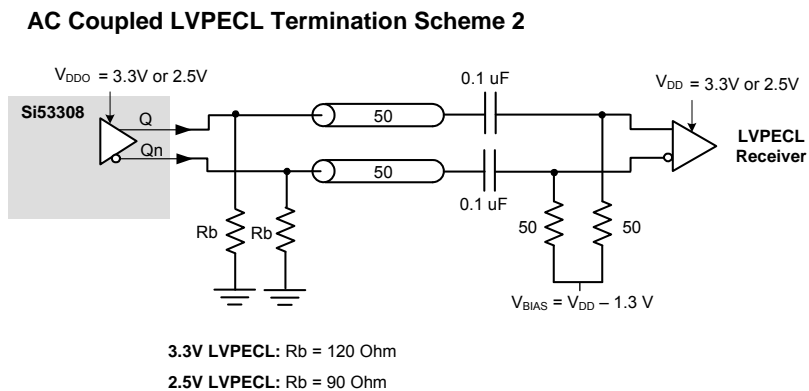
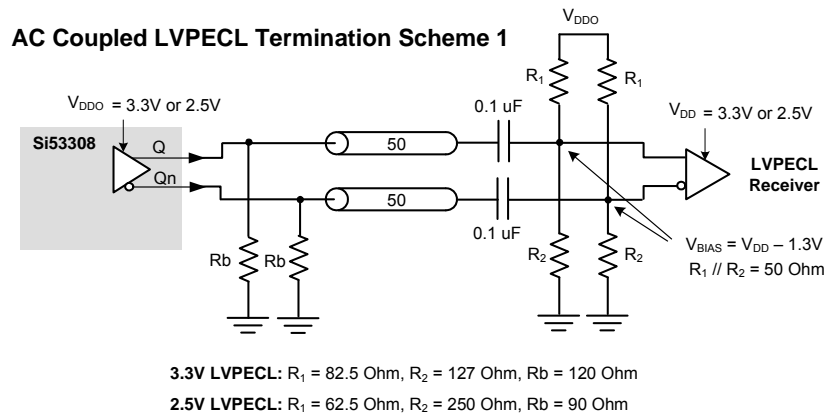
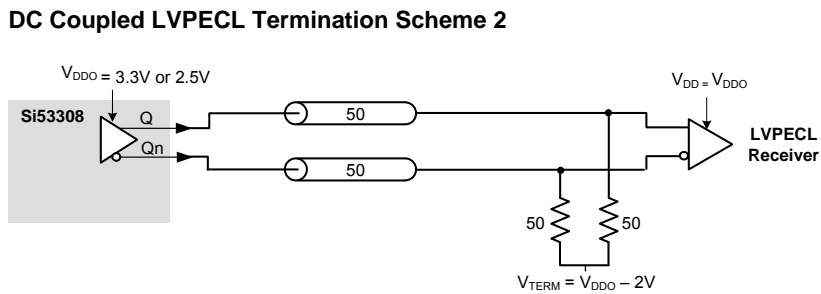
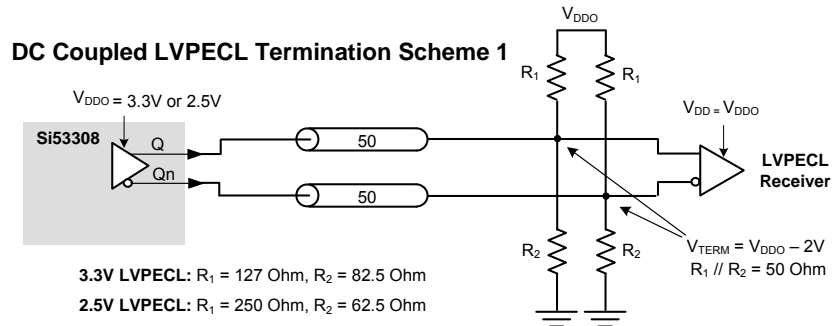
## 2.8. Power Supply ( $V_{DD}$ and $V_{DDOX}$ )

The device includes separate core ( $V_{DD}$ ) and output driver supplies ( $V_{DDOX}$ ). This feature allows the core to operate at a lower voltage than  $V_{DDO}$ , reducing current consumption in mixed supply applications. The core  $V_{DD}$  supports 3.3 V, 2.5 V, or 1.8 V. Each output bank has its own  $V_{DDOX}$  supply, supporting 3.3 V, 2.5 V, or 1.8 V.

$V_{DDOA}$  is the power supply for Q0,  $\overline{Q0}$ , Q1,  $\overline{Q1}$ , Q2,  $\overline{Q2}$  and  $V_{DDOB}$  is the power supply for Q3,  $\overline{Q3}$ , Q4,  $\overline{Q4}$ , Q5, Q5, as shown in Figure 2, "Functional Block Diagram,".

## 2.9. Output Clock Termination Options

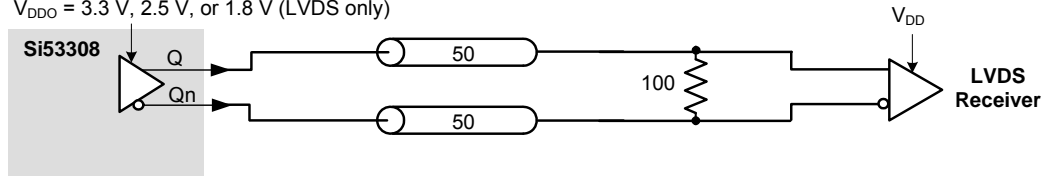
The recommended output clock termination options are shown below. Unused outputs can be left floating. Do not short unused outputs to ground.



**Figure 7. LVPECL Output Termination**

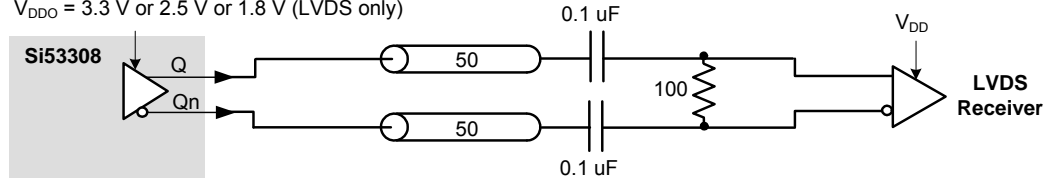
### DC Coupled LVDS and Low-Power LVPECL Termination

$V_{DDO} = 3.3\text{ V}, 2.5\text{ V}, \text{ or } 1.8\text{ V}$  (LVDS only)



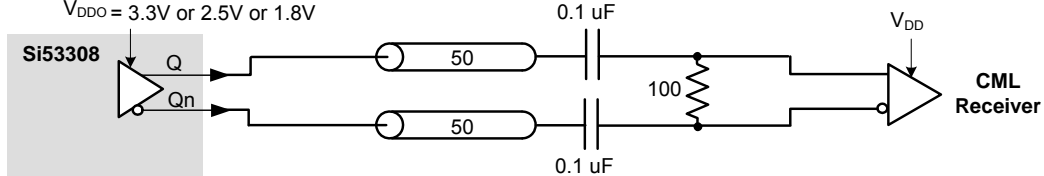
### AC Coupled LVDS and Low-Power LVPECL Termination

$V_{DDO} = 3.3\text{ V or } 2.5\text{ V or } 1.8\text{ V}$  (LVDS only)



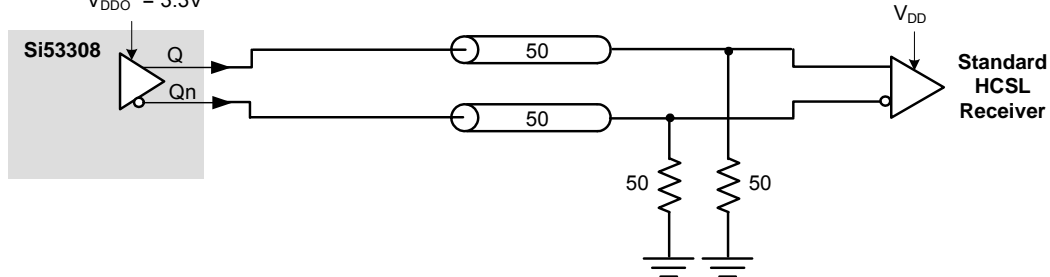
### AC Coupled CML Termination

$V_{DDO} = 3.3\text{ V or } 2.5\text{ V or } 1.8\text{ V}$



### DC Coupled HCSL Receiver Termination

$V_{DDO} = 3.3\text{ V}$



### DC Coupled HCSL Optimized Source Termination

$V_{DDO} = 3.3\text{ V}$

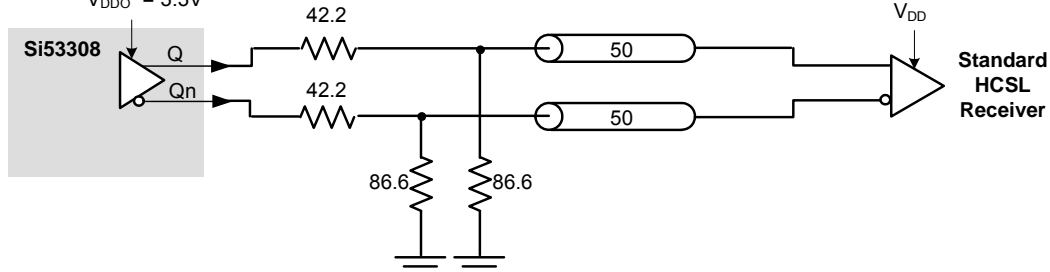


Figure 8. LVDS, CML, HCSL, and Low-Power LVPECL Output Termination

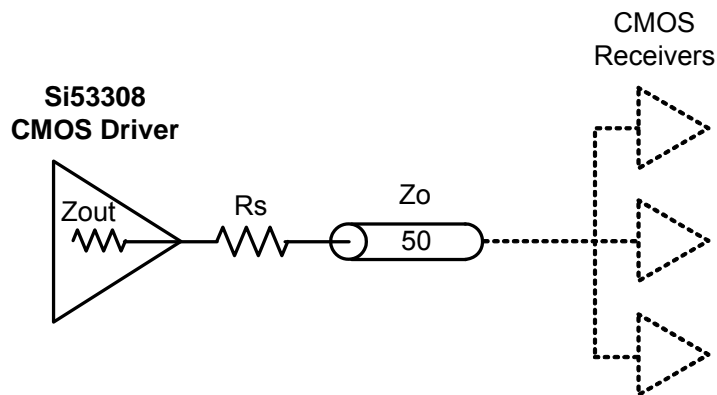


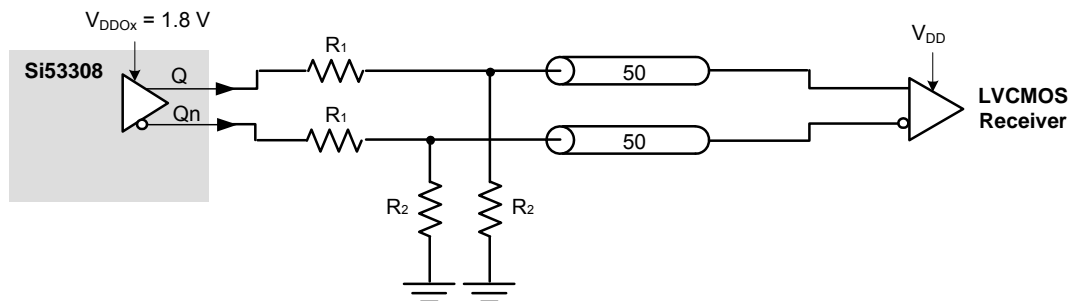
Figure 9. LVC MOS Output Termination

Table 20. Recommended LVC MOS  $R_S$  Series Termination

SFOUTX[1]	SFOUTX[0]	$R_S$ (ohms)		
		3.3 V	2.5 V	1.8 V
0	1	33	33	33
1	0	33	33	33
1	1	33	33	0
Open	0	0	0	0

### 2.9.1. LVC MOS Output Termination To Support 1.5 V and 1.2 V

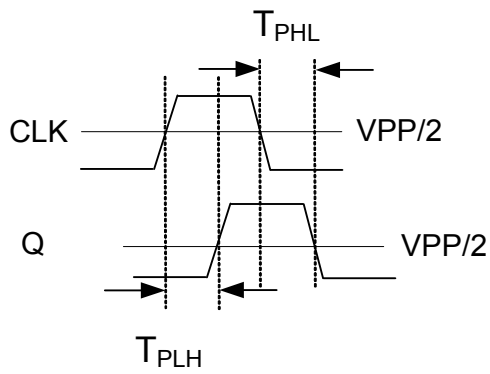
LVC MOS clock outputs are natively supported at 1.8, 2.5, and 3.3 V. However, 1.2 V and 1.5 V LVC MOS clock outputs can be supported via a simple resistor divider network that will translate the buffer's 1.8 V output to a lower voltage, as shown in Figure 10 below.



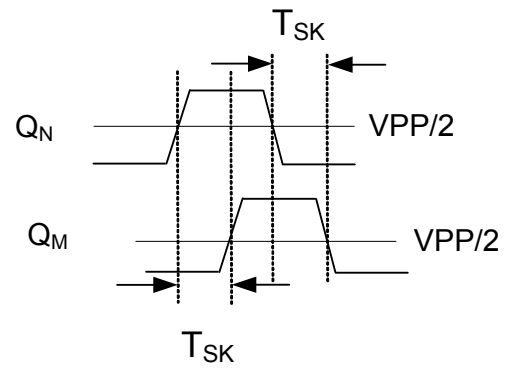
1.5 V LVC MOS:  $R_1 = 43$  ohms,  $R_2 = 300$  ohms,  $I_{OUT} = 12$  mA  
 1.2 V LVC MOS:  $R_1 = 58$  ohms,  $R_2 = 150$  ohms,  $I_{OUT} = 12$  mA

Figure 10. 1.5 V and 1.2 V LVC MOS Low-Voltage Output Termination

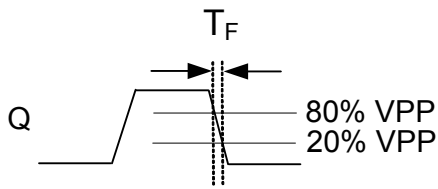
## 2.10. AC Timing Waveforms



Propagation Delay



Output-Output Skew



Rise/Fall Time

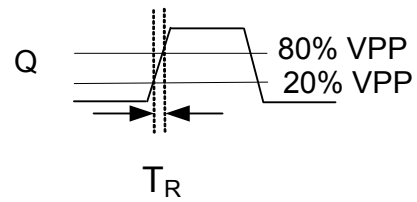


Figure 11. AC Waveforms

## 2.11. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

**Source Jitter:** Reference clock phase noise.

**Total Jitter (SE):** Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

**Total Jitter (Diff'I):** Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 10.

**Note:** To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



**Important:** See AN925 for additional information on the dependence of measured additive jitter on the input source jitter.

Figure 12. Source Jitter (156.25 MHz)

Table 21. Source Jitter (156.25 MHz)

Frequency (MHz)	Diff'I Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'I) (fs)	Additive Jitter (Diff'I) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

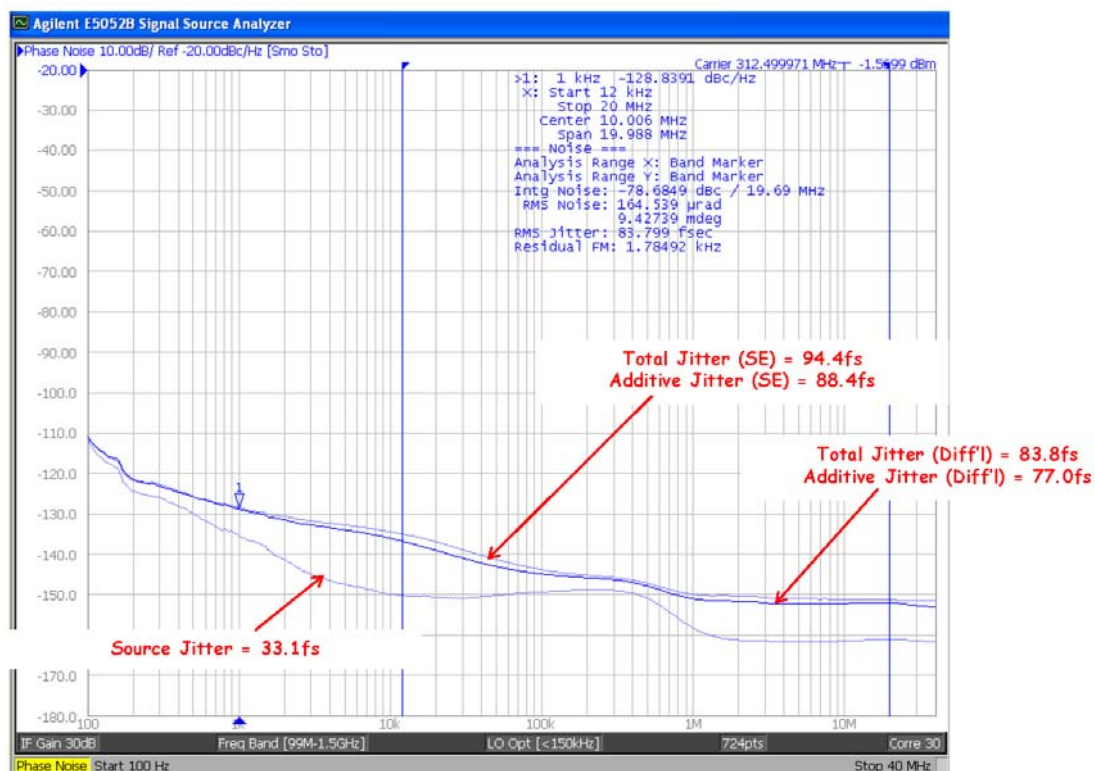


Figure 13. Single-Ended Total Jitter (312.5 MHz)

Table 22. Single-Ended Total Jitter (312.5 MHz)

Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
312.5	1.0	33.1	94.4	88.4	83.8	77.0

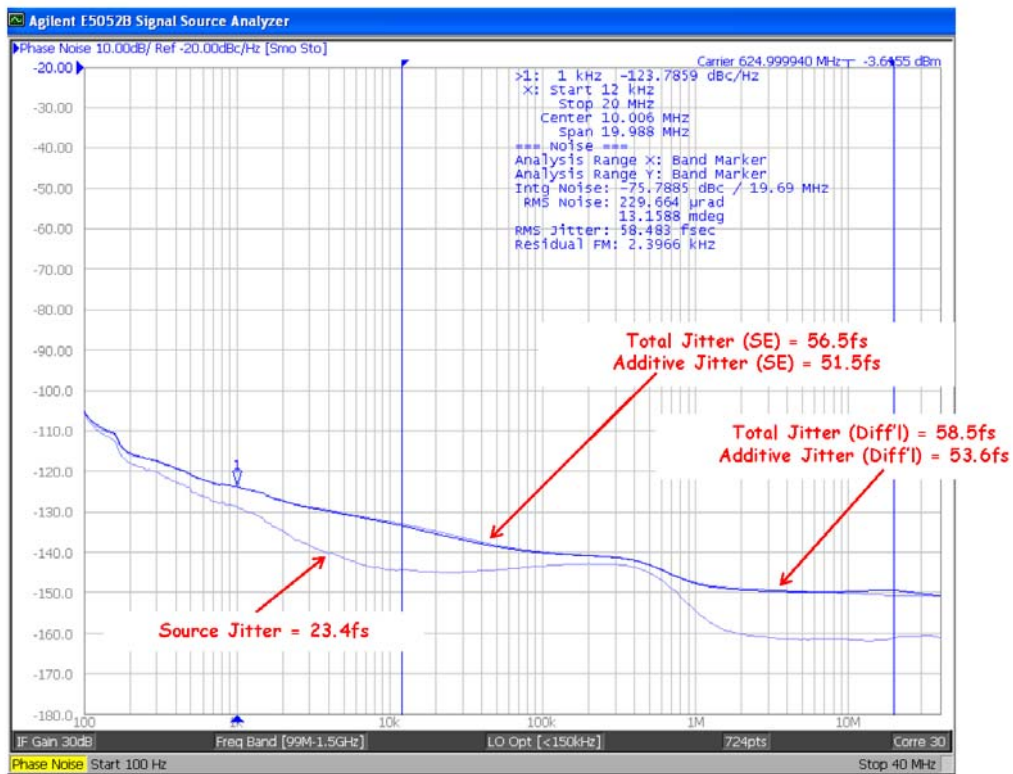


Figure 14. Differential Total Jitter (625 MHz)

Table 23. Single-Ended Total Jitter (312.5 MHz)

Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
625	1.0	23.4	56.5	51.5	58.5	53.6



## 2.12. Input Noise Isolation

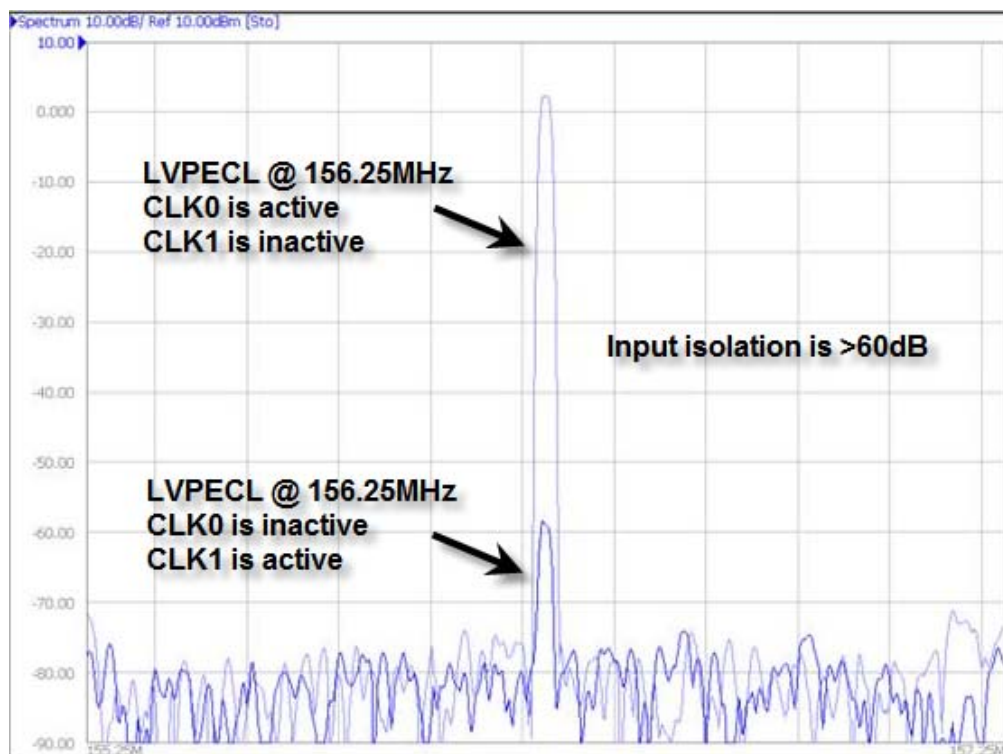
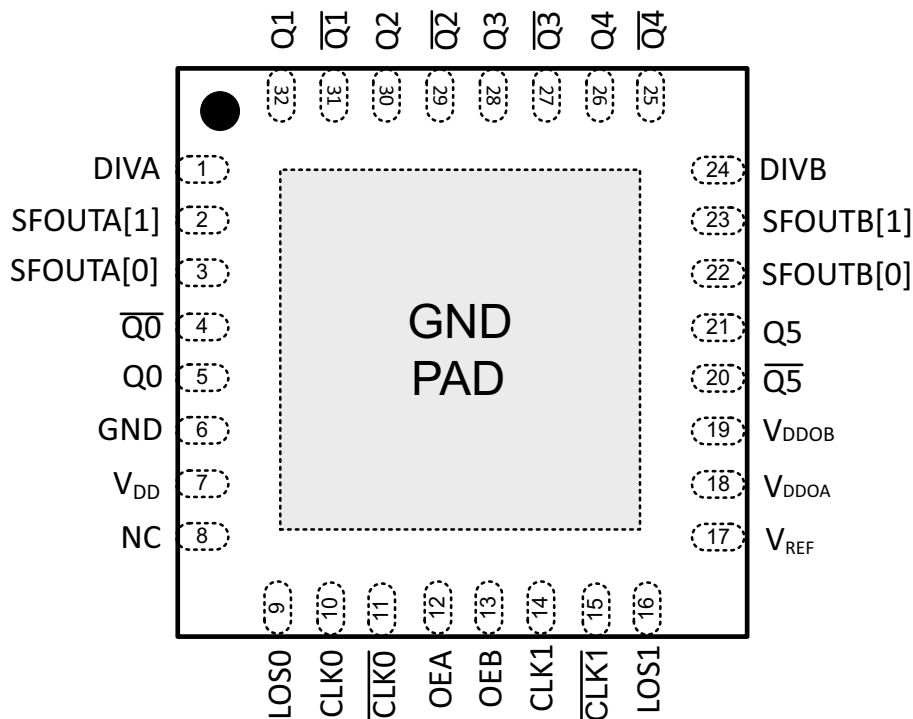


Figure 15. Input Noise Isolation

## 2.13. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

## 3. Pin Description: 32-Pin QFN



**Table 24. Pin Descriptions**

Pin	Name	Type*	Description
1	DIVA	I	Output divider control pin for Bank A. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD.
2	SFOUTA[1]	I	Output signal format control pin for Bank A. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD.
3	SFOUTA[0]	I	Output signal format control pin for Bank A. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD.
4	$\overline{Q0}$	O	Output clock 0 (complement).
5	Q0	O	Output clock 0.
6	GND	GND	Ground.
7	VDD	P	Core voltage supply. Bypass with 1.0 $\mu$ F capacitor and place close to the VDD pin as possible.

\*Note: Pin types are: I = input, O = output, P = power, GND = ground.

Table 24. Pin Descriptions (Continued)

Pin	Name	Type*	Description
8	NC	I	No connect.
9	LOS0	O	The LOS0 status pin indicates whether a clock is present (LOS0 = 0) or not present (LOS0 = 1) at the CLK0 pin.
10	CLK0	I	Input clock 0.
11	$\overline{\text{CLK0}}$	I	Input clock 0 (complement). When CLK0 is driven by a single-ended input, connect $\overline{\text{CLK0}}$ to VDD/2.
12	OEA	I	Output enable—Bank A. When OE = high, the Bank A outputs are enabled. When OE = low, Q is held low and $\overline{Q}$ is held high for differential formats. For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low. OEA contains an internal pull-up resistor.
13	OEB	I	Output enable—Bank B. When OE = high, the Bank B outputs are enabled. When OE = low, Q is held low and $\overline{Q}$ is held high for differential formats. For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low. OEB contains an internal pull-up resistor.
14	CLK1	I	Input clock 1.
15	$\overline{\text{CLK1}}$	I	Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect $\overline{\text{CLK1}}$ to VDD/2.
16	LOS1	O	The LOS1 status pin indicates whether a clock is present (LOS1 = 0) or not present (LOS1 = 1) at the CLK1 pin.
17	V <sub>REF</sub>	O	Reference voltage.
18	V <sub>DDOA</sub>	P	Output Clock Voltage Supply—Bank A (Outputs: Q0 to Q2). Bypass with 1.0 $\mu$ F capacitor and place as close to the V <sub>DDOA</sub> pin as possible.
19	V <sub>DDOB</sub>	P	Output Clock Voltage Supply—Bank B (Outputs: Q3 to Q5). Bypass with 1.0 $\mu$ F capacitor and place as close to the V <sub>DDOB</sub> pin as possible.
20	$\overline{\text{Q5}}$	O	Output clock 5 (complement).
21	Q5	O	Output clock 5.
22	SFOUTB[0]	I	Output signal format control pin for Bank B. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V <sub>DD</sub> .
23	SFOUTB[1]	I	Output signal format control pin for Bank B. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V <sub>DD</sub> .

\*Note: Pin types are: I = input, O = output, P = power, GND = ground.

**Table 24. Pin Descriptions (Continued)**

Pin	Name	Type*	Description
24	DIVB	I	Output divider control pin for Bank B. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD.
25	$\overline{Q4}$	O	Output clock 4 (complement).
26	Q4	O	Output clock 4.
27	$\overline{Q3}$	O	Output clock 3 (complement).
28	Q3	O	Output clock 3.
29	$\overline{Q2}$	O	Output clock 2 (complement).
30	Q2	O	Output clock 2.
31	$\overline{Q1}$	O	Output clock 1 (complement).
32	Q1	O	Output clock 1.
GND Pad	GND	GND	Ground Pad. Power supply ground and thermal relief.

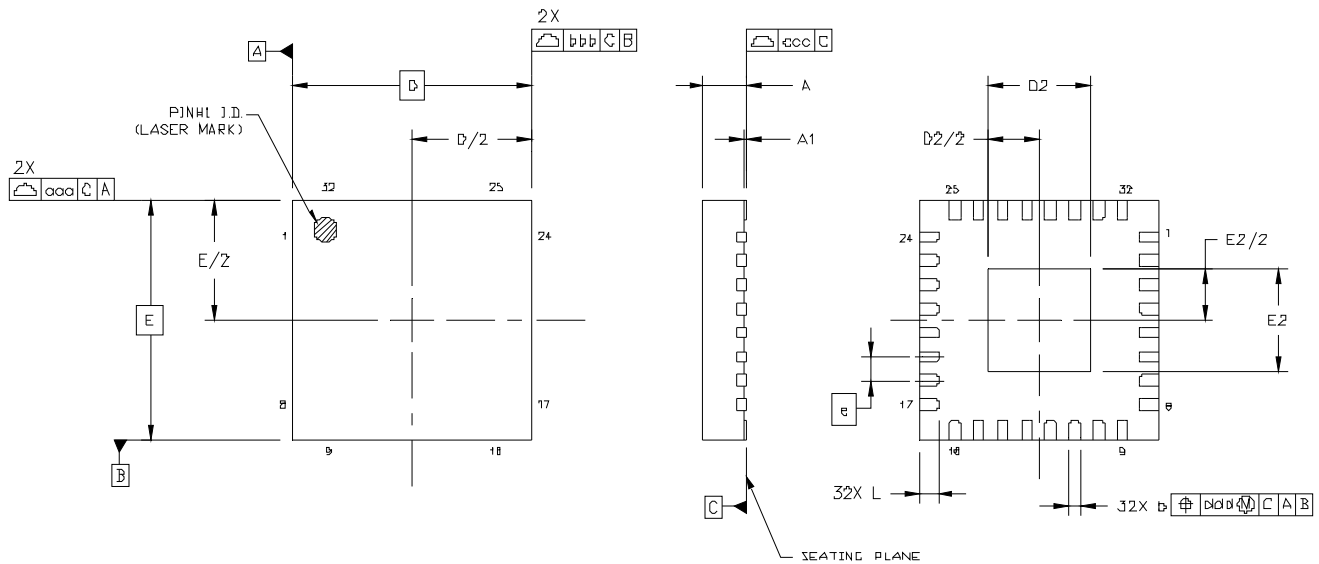
**\*Note:** Pin types are: I = input, O = output, P = power, GND = ground.

**4. Ordering Guide**

<b>Part Number</b>	<b>Package</b>	<b>PB-Free, ROHS-6</b>	<b>Temperature</b>
Si53308-B-GM	32-QFN	Yes	-40 to 85 °C
Si53301/4-EVB	NA	Yes	-40 to 85 °C

## 5. Package Outline

### 5.1. 5x5 mm 32-QFN Package Diagram



**Figure 16. Si53308 5x5 mm 32-QFN Package Diagram**

**Table 25. Package Dimensions**

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	5.00 BSC		
D2	2.00	2.15	2.30
e	0.50 BSC		
E	5.00 BSC		
E2	2.00	2.15	2.30
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
<b>Notes:</b>			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. This drawing conforms to the JEDEC Solid State Outline MO-220.			

## 6. PCB Land Pattern

### 6.1. 5x5 mm 32-QFN Package Land Pattern

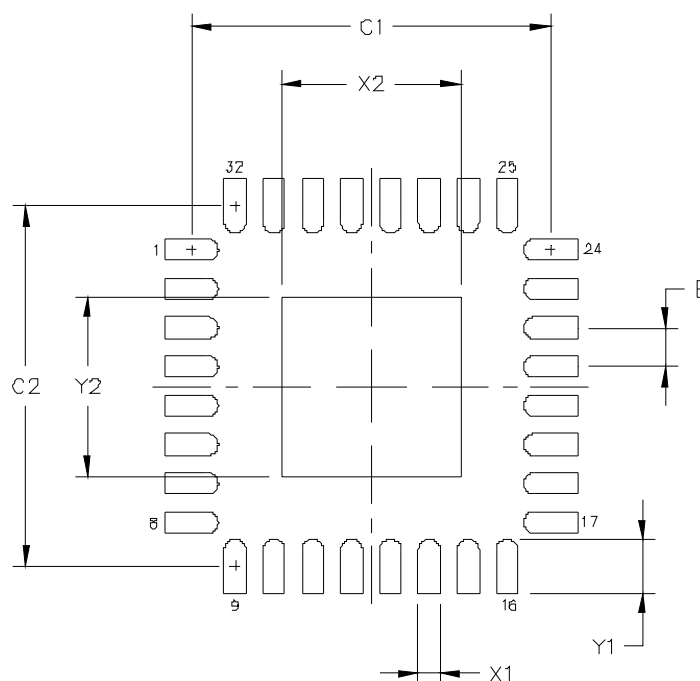


Figure 17. Si53308 5x5 mm 32-QFN Package Land Pattern

Table 26. PCB Land Pattern

Dimension	Min	Max	Dimension	Min	Max
C1	4.52	4.62	X2	2.20	2.30
C2	4.52	4.62	Y1	0.59	0.69
E	0.50 BSC		Y2	2.20	2.30
X1	0.20	0.30			

#### Notes:

##### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

##### Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

##### Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

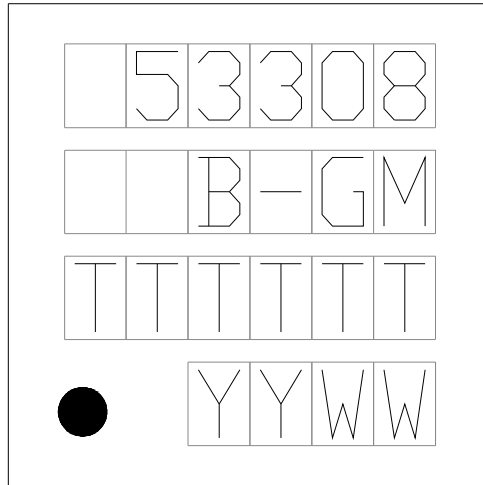
##### Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# Si53308

## 7. Top Marking

### 7.1. Si53308 Top Marking



### 7.2. Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	2.0 Point (28 mils) Center-Justified	
<b>Line 1 Marking:</b>	Device Part Number	<b>53308</b>
<b>Line 2 Marking:</b>	Device Revision/Type	<b>B-GM</b>
<b>Line 3 Marking:</b>	TTTTTT = Mfg Code	Manufacturing Code.
<b>Line 4 Marking</b>	Circle = 0.5 mm Diameter Lower-Left Justified	Pin 1 Identifier
	YY = Year WW = Work Week	Corresponds to the year and work week of the mold date.



## DOCUMENT CHANGE LIST

### Revision 0.9 to Revision 1.0

March 3, 2016

- Updated Functional Block Diagram.
- Updated Table 3, Table 10, and Table 17.
- Updated Table 24, “Pin Descriptions,” on page 26.
- Updated Figure 10.



## ClockBuilder Pro

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