QUAD DIGITAL ISOLATORS WITH DC-DC CONVERTER

Features

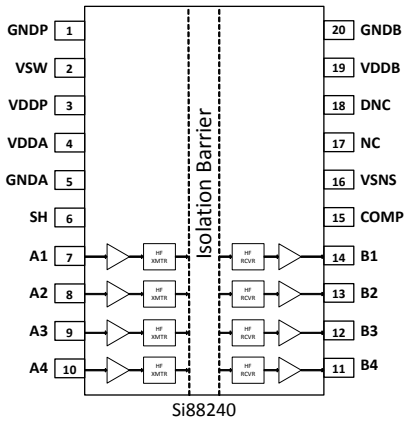
- High-speed isolators with integrated dc-dc converter
- Fully-integrated secondary sensing feedback-controlled converter with dithering for low EMI
- dc-dc converter peak efficiency of 83% with external power switch
- Up to 5 W isolated power with external power switch
- Options include dc-dc shutdown, frequency control, and soft start
- Standard Voltage Conversion
  - 3/5 V to isolated 3/5 V
  - 24 V to isolated 3/5 V supported
- Precise timing on digital isolators
  - 0–100 Mbps
  - 18 ns typical prop delay
- Highly-reliable: 100 year lifetime
- High electromagnetic immunity and ultra-low emissions
- RoHS compliant packages
  - SOIC-20 wide body
  - SOIC-24 wide body
- Isolation of up to 5000 Vrms
- High transient immunity of 100 kV/µs (typical)
- AEC-Q100 qualified
- Wide temp range
  - –40 to +125 °C

Ordering Information:

See page 38.

Pin Assignments

See page 33



Patents pending

Applications

- Industrial automation systems
- Hybrid electric and electric vehicles
- Isolated power supplies
- Inverters
- Data acquisition
- Motor control
- PLCs, distributed control systems

Safety Approval (Pending)

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
  - CSA component notice 5A approval
- VDE certification conformity
  - VDE 0884-10
- CQC certification approval
  - GB4943.1

Description

The Si88xx integrates Silicon Labs' proven digital isolator technology with an on-chip isolated dc-dc converter that provides regulated output voltages of 3.3 or 5.0 V (or >5 V with external components) at peak output power levels of up to 5 W. These devices provide up to four digital channels. The dc-dc converter has user-adjustable frequency for minimizing emissions, a soft-start function for safety, a shut-down option and loop compensation. The device requires only minimal passive components and a miniature transformer.

The ultra-low-power digital isolation channels offer substantial data rate, propagation delay, size and reliability advantages over legacy isolation technologies. Data rates up to 100 Mbps max are supported, and all devices achieve propagation delays of only 23 ns max. Ordering options include a choice of dc-dc converter features, isolation channel configurations and a fail-safe mode. All products are certified by UL, CSA, VDE, and CQC.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	–40	25	125	°C
Power Input Voltage	VDDP	3.0	—	5.5	V
Supply Voltage	VDDA	3.0	—	5.5	V
	VDDB	3.0	—	5.5	V
***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.					

Table 2. Electrical Characteristics[1]

V_{IN} = 24 V; V_{DDA} = 4.3 V (see Figure 3) for all Si8844x/64x; V_{DDA} = V_{DDP} = 3.0 to 5.5 V (see Figure 2) for all Si8824x/34x; T_A = –40 to 125 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC/DC Converter						
Switching Frequency Si8824x, Si8844x	FSW			250		kHz
Switching Frequency Si8834x, Si8864x	FSW	RFSW = 23.3 kΩ FSW = 1025.5/(RFSW x CSS) CSS = 220 nF (see Figure 9) (1% tolerance on BOM)	180	200	220	kHz
		RFSW = 9.3 kΩ FSW = 1025.5/(RFSW x CSS) CSS = 220 nF (see Figure 9) (1% tolerance on BOM)	450	500	550	kHz
		RFSW = 5.18 kΩ, CSS = 220 nF (see Figure 9)	810	900	990	kHz
VSNS voltage	VSNS	ILOAD = 0 A	1.002	1.05	1.097	V
VSNS current offset	I_{offset}		–500	—	500	nA

Notes:
1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

V_{IN} = 24 V; V_{DDA} = 4.3 V (see Figure 3) for all Si8844x/64x; V_{DDA} = V_{DDP} = 3.0 to 5.5 V (see Figure 2) for all Si8824x/34x; T_A = –40 to 125 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage Accuracy[2]		See Figure 2 ILOAD = 0 mA	–5	—	+5	%
Line Regulation	ΔVOUT(line)/ΔVDDP	See Figure 2 ILOAD = 50 mA VDDP varies from 4.5 to 5.5 V		1		mV/V
Load Regulation	ΔVOUT(load)/VOUT	See Figure 2 ILOAD = 50 to 400 mA		0.1		%
Output Voltage Ripple Si8824x, Si8834x Si8844x, Si8864x		ILOAD = 100 mA See Figure 2 See Figure 3		100		mV p-p
Turn-on overshoot	ΔVOUT(start)	See Figure 2 CIN = COUT = 0.1 µF in parallel with 10 µF, ILOAD = 0 A		2		%
Continuous Output Current Si8824x, Si8834x 5.0 V to 5.0 V 3.3 V to 3.3 V 3.3 V to 5.0 V 5.0 V to 3.3 V Si8844x, Si8864x 24.0 to 5.0 V 24.0 to 3.0 V	ILOAD(max)	 See Figure 2 See Figure 3		 400 400 250 550 1000 1500		mA
Cycle-by-cycle average current limit Si8824x, Si8834x	ILIM	See Figure 2 Output short circuited		3		A
No Load Supply Current IDDP Si8824x, Si8834x	IDDPQ_DCDC[3]	See Figure 2 VDDP = VDDA = 5 V		30		mA
No Load Supply Current IDDA Si8824x, Si8834x	IDDAQ_DCDC[4]	See Figure 2 VDDP = VDDA = 5 V		5.7		mA

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
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V_{IN} = 24 V; V_{DDA} = 4.3 V (see Figure 3) for all Si8844x/64x; V_{DDA} = V_{DDP} = 3.0 to 5.5 V (see Figure 2) for all Si8824x/34x; T_A = –40 to 125 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
No Load Supply Current IDDP Si8844x, Si8864x	IDDPQ_DCDC[3]	See Figure 3 VIN = 24 V		0.8		mA
No Load Supply Current IDDA Si8844x, Si8864x	IDDAQ_DCDC[4]	See Figure 3 VIN = 24 V		5.8		mA
Peak Efficiency Si8824x, Si8834x Si8844x, Si8864x	η	See Figure 2, 3		 78 83		%
Voltage Regulator Reference Voltage Si8844x, Si8864x	VREGA, VREGB	I_{REG} = 600 µA See Figure 30 for typical I–V curve		4.8		V
VREG tempco	K_{TVREG}			–0.43		mV/°C
VREG input current	I_{REG}		350	—	950	µA
Soft Start Time, Full Load Si8824x, Si8844x Si8834x, Si8864x	t_{SST}	See Figures 25 through 28 for typical soft start times over load conditions.		 25 50		ms
Restart Delay from fault event	tOTP			21		s
Digital Isolator						
VDD Undervoltage Threshold	VDDUV+	VDDA, VDDB rising		2.7		V
VDD Undervoltage Threshold	VDDUV–	VDDA, VDDB falling		2.6		V
VDD Undervoltage Hysteresis	VDD_{HYS}			100		mV
Positive-Going Input Threshold	VT+	All inputs rising		1.67		V

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

V_{IN} = 24 V; V_{DDA} = 4.3 V (see Figure 3) for all Si8844x/64x; V_{DDA} = V_{DDP} = 3.0 to 5.5 V (see Figure 2) for all Si8824x/34x; T_A = –40 to 125 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative-Going Input Threshold	VT–	All inputs falling		1.23		V
Input Hysteresis	V_{HYS}			0.44		V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DDA}, V_{DDB} – 0.4	—	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	—	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance	Z_O		—	50	—	Ω
Supply Current, C_{LOAD} = 15 pF						
DC, VDDx = 3.3 V ± 10%						
Si88x40						
V_{DDA}		All inputs = 0	—	12.9		mA
V_{DDB}		All inputs = 0	—	5.4		
V_{DDA}		All inputs = 1	—	5.1		
V_{DDB}		All inputs = 1	—	5.3		
Si88x41						
V_{DDA}		All inputs = 0	—	10.9		mA
V_{DDB}		All inputs = 0	—	6.8		
V_{DDA}		All inputs = 1	—	5.6		
V_{DDB}		All inputs = 1	—	5.1		
Si88x42						
V_{DDA}		All inputs = 0	—	9.7		mA
V_{DDB}		All inputs = 0	—	7.8		
V_{DDA}		All inputs = 1	—	5.9		
V_{DDB}		All inputs = 1	—	4.3		

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si88x43						
V_{DDA}		All inputs = 0	—	8.5		mA
V_{DDB}		All inputs = 0	—	9.3		
V_{DDA}		All inputs = 1	—	6.5		
V_{DDB}		All inputs = 1	—	3.9		
Si88x44						mA
V_{DDA}		All inputs = 0	—	6.6		
V_{DDB}		All inputs = 0	—	10.6		
V_{DDA}		All inputs = 1	—	6.5		
V_{DDB}		All inputs = 1	—	3.6		
1 Mbps, VDDx = 3.3 V ± 10% (All Inputs = 500 kHz Square Wave, C_{LOAD} = 15 pF)						
Si88x40						mA
V_{DDA}			—	8.9		
V_{DDB}			—	5.4		
Si88x41						mA
V_{DDA}			—	8.3		
V_{DDB}			—	6.0		
Si88x42						mA
V_{DDA}			—	7.9		
V_{DDB}			—	6.1		
Si88x43						mA
V_{DDA}			—	7.6		
V_{DDB}			—	6.7		
Si88x44						mA
V_{DDA}			—	6.7		
V_{DDB}			—	7.1		
100 Mbps, VDDx = 3.3 V ± 10% (All Inputs = 50 MHz Square Wave, C_{LOAD} = 15 pF)						
Si88x40						mA
V_{DDA}			—	8.7		
V_{DDB}			—	19.2		

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

V_{IN} = 24 V; V_{DDA} = 4.3 V (see Figure 3) for all Si8844x/64x; V_{DDA} = V_{DDP} = 3.0 to 5.5 V (see Figure 2) for all Si8824x/34x; T_A = –40 to 125 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si88x41						mA
V_{DDA}			—	12.7		
V_{DDB}			—	16.6		
Si88x42						mA
V_{DDA}			—	15.6		
V_{DDB}			—	13.6		
Si88x43						mA
V_{DDA}			—	18.7		
V_{DDB}			—	11.0		
Si88x44						mA
V_{DDA}			—	21.6		
V_{DDB}			—	6.9		

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

V_{IN} = 24 V; V_{DDA} = 4.3 V (see Figure 3) for all Si8844x/64x; V_{DDA} = V_{DDP} = 3.0 to 5.5 V (see Figure 2) for all Si8824x/34x; T_A = –40 to 125 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC, VDDx = 5 V ± 10%						
Si88x40						
V_{DDA}		All inputs = 0	—	13.1		mA
V_{DDB}		All inputs = 0	—	5.6		
V_{DDA}		All inputs = 1	—	5.2		
V_{DDB}		All inputs = 1	—	5.4		
Si88x41						
V_{DDA}		All inputs = 0	—	11.1		mA
V_{DDB}		All inputs = 0	—	6.9		
V_{DDA}		All inputs = 1	—	5.7		
V_{DDB}		All inputs = 1	—	5.2		
Si88x42						
V_{DDA}		All inputs = 0	—	10.1		mA
V_{DDB}		All inputs = 0	—	7.9		
V_{DDA}		All inputs = 1	—	6.2		
V_{DDB}		All inputs = 1	—	4.4		
Si88x43						
V_{DDA}		All inputs = 0	—	8.6		mA
V_{DDB}		All inputs = 0	—	9.2		
V_{DDA}		All inputs = 1	—	6.6		
V_{DDB}		All inputs = 1	—	3.9		
Si88x44						
V_{DDA}		All inputs = 0	—	6.8		mA
V_{DDB}		All inputs = 0	—	11.0		
V_{DDA}		All inputs = 1	—	6.7		
V_{DDB}		All inputs = 1	—	3.8		
1 Mbps, VDDx = 5 V ± 10% (All Inputs = 500 kHz Square Wave, C_{LOAD} = 15 pF)						
Si88x40						mA
V_{DDA}			—	9.1		
V_{DDB}			—	5.8		

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
4. VDDA current needed for dc-dc circuits.
5. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
6. tPSK(P-P) is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
7. Start-up time is the time period from when the UVLO threshold is exceeded to valid data at the output.

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si88x41 V_{DDA} V_{DDB}			 — —	 8.4 6.3		mA
Si88x42 V_{DDA} V_{DDB}			 — —	 8.2 6.2		mA
Si88x43 V_{DDA} V_{DDB}			 — —	 7.8 6.7		mA
Si88x44 V_{DDA} V_{DDB}			 — —	 6.9 7.4		mA
100 Mbps, VDDx = 5 V ± 10% (All Inputs = 50 MHz Square Wave, C_{LOAD} = 15 pF)						
Si88x40 V_{DDA} V_{DDB}			 — —	 8.2 26.2		mA
Si88x41 V_{DDA} V_{DDB}			 — —	 14.7 22.0		mA
Si88x42 V_{DDA} V_{DDB}			 — —	 18.9 16.5		mA
Si88x43 V_{DDA} V_{DDB}			 — —	 24.0 11.7		mA
Si88x44 V_{DDA} V_{DDB}				 28.1 6.6		mA
Timing Characteristics						
Data Rate			0	—	100	Mbps

Notes:

1. Over recommended operating conditions as noted in Table 1.
2. VOUT = VSNS x (1 + R1/R2) + R1 x I_{offset}
3. VDDP current needed for dc-dc circuits.
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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width			10	—	—	ns
Propagation Delay	t_{PHL}	See Figure 1 VDDx = 3.3 V	—	17.8	—	ns
Propagation Delay	t_{PLH}	See Figure 1 VDDx = 3.3 V	—	14.5	—	ns
Propagation Delay	t_{PHL}	See Figure 1 VDDx = 5.0 V	—	17.5	—	ns
Propagation Delay	t_{PLH}	See Figure 1 VDDx = 5.0 V	—	12.6	—	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1 VDDx = 3.3 V	—	3.4	—	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1 VDDx = 5.0 V	—	4.8	—	ns
Propagation Delay Skew[6]	$t_{PSK(P-P)}$		—	2.0	—	ns
Channel-Channel Skew	t_{PSK}		—	1.0	—	ns
Output Rise Time	t_r	C_{LOAD} = 15 pF	—	2.5	—	ns
Output Fall Time	t_f	C_{LOAD} = 15 pF	—	2.5	—	ns
Common Mode Transient Immunity	CMTI	V_I = VDDx or 0 V V_{CM} = 1500 V See Figure 4	40	100	—	kV/µs
Startup Time[7]	t_{SU}		—	55	—	µs

Notes:

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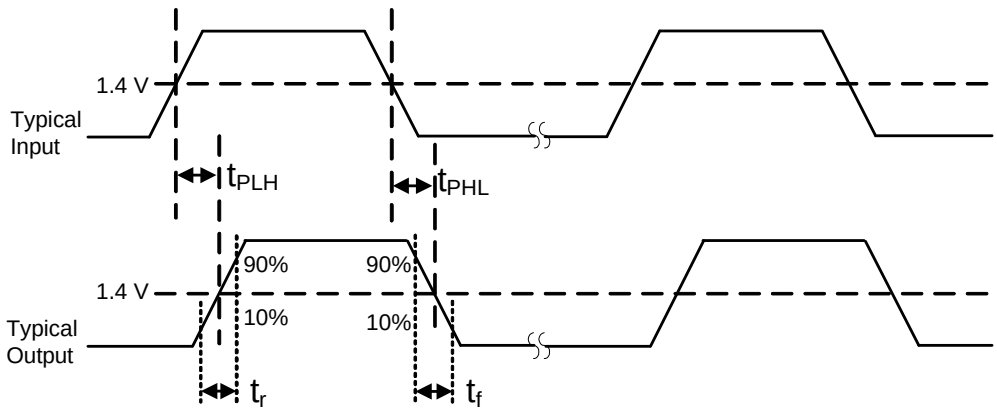


Figure 1. Propagation Delay Timing for Digital Channels

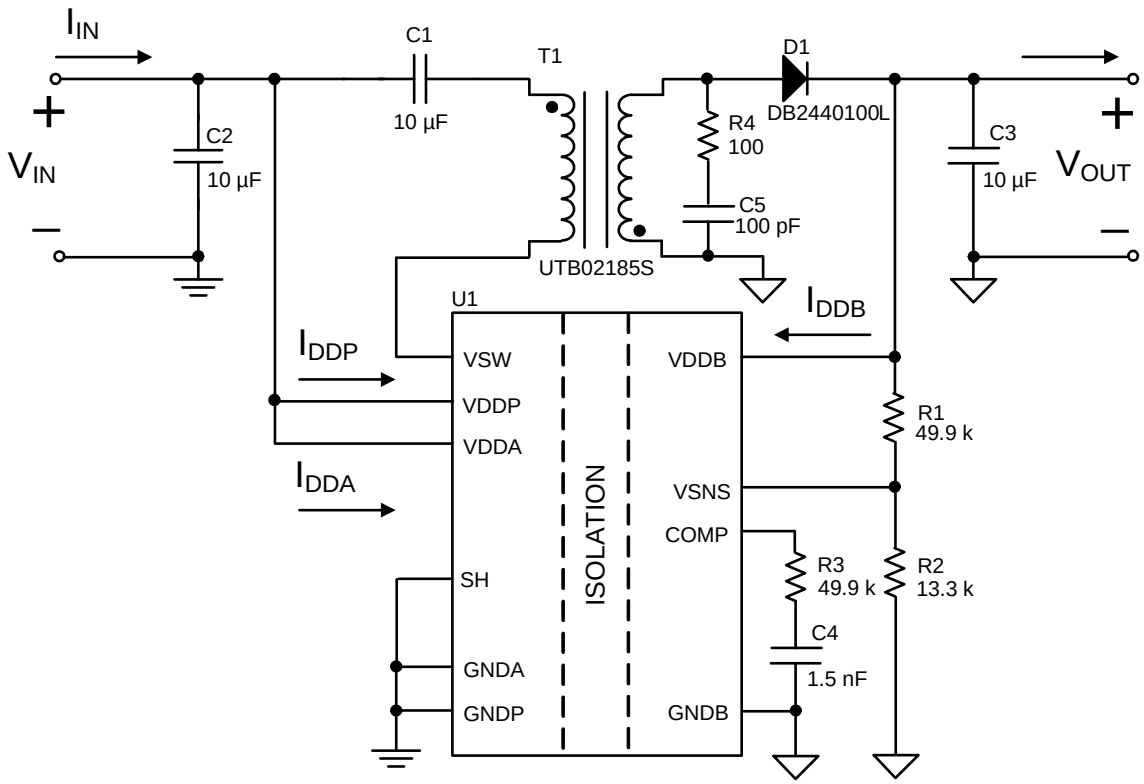


Figure 2. Measurement Circuit for Converter Efficiency and Regulation for Si882xx, Si883xx

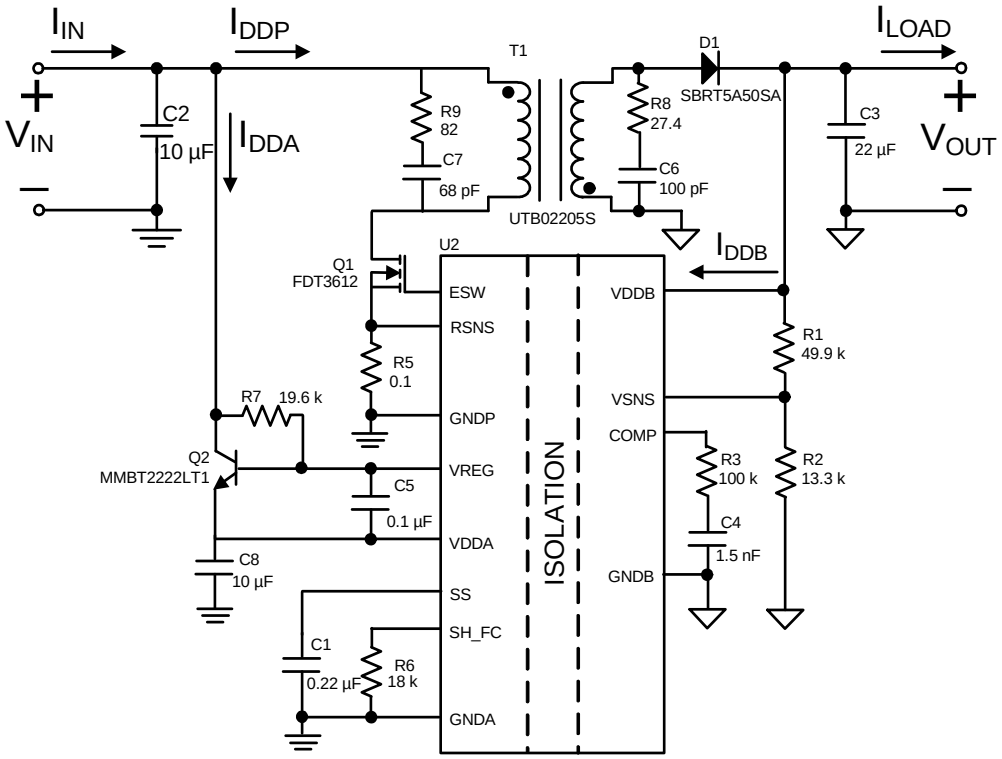


Figure 3. Measurement Circuit for Converter Efficiency and Regulation for Si884xx, Si886xx

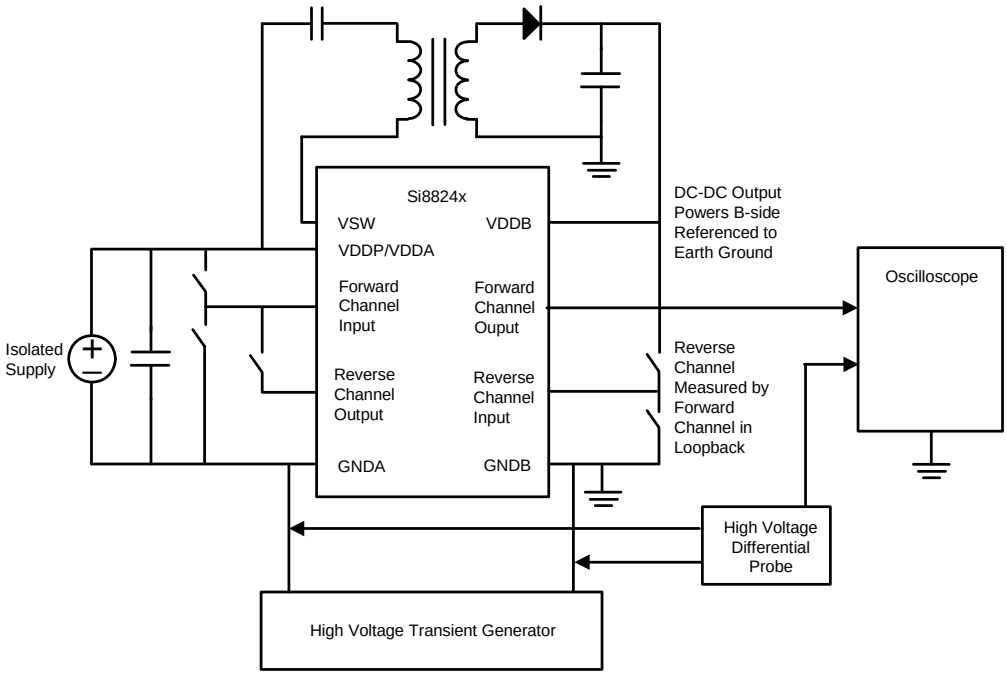


Figure 4. Common-Mode Transient Immunity Test Circuit

Table 3. Regulatory Information[1,2]

CSA
The Si88xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE
The Si88xx is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001.
VDE 0884-10: Up to 891 V_{peak} for basic insulation working voltage.
UL
The Si88xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si88xx is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Notes: **1.** Regulatory Certifications apply to 5 kVRMS rated devices which are production tested to 6.0 kVRMS for 1 sec. **2.** All certifications are pending.

Table 4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			WB SOIC-20 WB SOIC-24	
Nominal Air Gap (Clearance)	L(1O1)		8.0[1]	mm
Nominal External Tracking (Creepage)	L(1O2)		8.0[1]	mm
Minimum Internal Gap (Internal Clearance)			0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.4	pF
Input Capacitance[3]	C_I		4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-20 and WB SOIC-24 packages. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 7.6 mm minimum for the WB SOIC-20 and WB SOIC-24 packages.
2. To determine resistance and capacitance, the Si88xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input to ground.

Table 5. IEC 60664-1 (VDE 0884-10) Ratings

Parameter	Test Condition	Specification
		WB SOIC-20 WB SOIC-24
Basic Isolation Group	Material Group	I
Installation Classification	Rate Mains Voltages ≤150 V_{RMS}	I–IV
	Rate Mains Voltages ≤300 V_{RMS}	I–IV
	Rate Mains Voltages ≤400 V_{RMS}	I–III
	Rate Mains Voltages ≤600 V_{RMS}	I–III

Table 6. VDE 0884-10 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic	Unit
			WB SOIC-20 WB SOIC-24	
Maximum Working Insulation Voltage	V_{IORM}		891	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si88xx provides a climate classification of 40/125/21.

Table 7. IEC Safety Limiting Values*

Parameter	Symbol	Test Condition	WB SOIC-20	Unit
Case Temperature	T_S		150	°C
Safety Input Current	I_S	θ_{JA} = 55 °C/W (WB SOIC-20), V_{DDA} = 5.5 V, T_J = 150 °C, T_A = 25 °C	413	mA
Device Power Dissipation	P_D		2.27	W

***Note:** Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 3.

Table 8. Thermal Characteristics

Parameter	Symbol	WB SOIC-20	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	55	°C/W

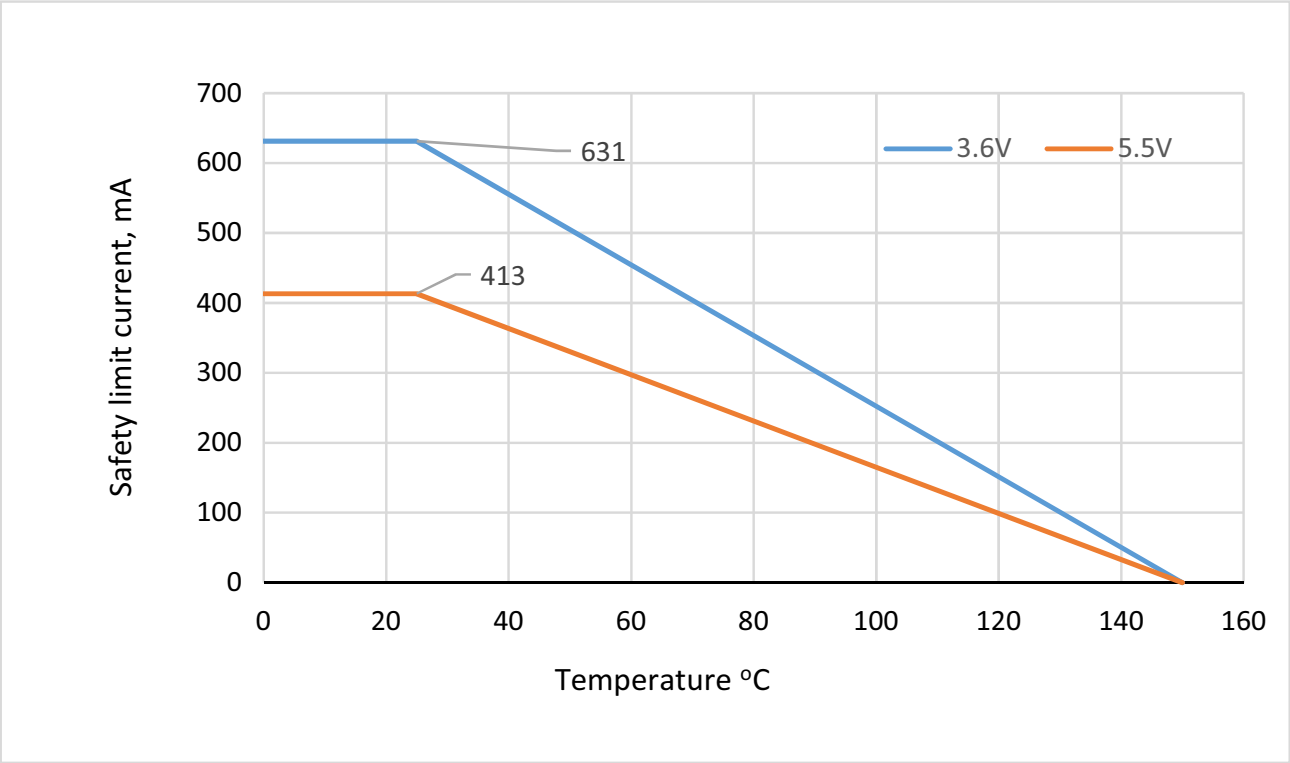


Figure 5. WB SOIC-20 Thermal Derating Curve*

***Note:** Values are not final and are subject to change. Dependence of Safety Limiting Values with Case Temperature per VDE 0884-10.

Table 9. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Junction Temperature	T_J	—	+150	°C
Input-side Supply Voltage	VDDA VDDP	–0.6	6.0	V
Output supply	VDDB	–0.6	6.0	V
Voltage on any Pin with respect to Ground	VIN	–0.5	VDD + 0.5	V
Output Drive Current per Channel	I_O		10	mA
Input Current for VREGA, VREGB	I_{REG}	—	1	mA
Lead Solder Temperature (10 s)		—	260	°C
ESD per AEC-Q100	HBM	—	4	kV
	CDM	—	2	kV
Maximum Isolation (Input to Output) (1 sec) WB SOIC-20, WB SOIC-24		—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.

2. Functional Description

2.1. Theory of Operation

The Si88xx family of products is capable of transmitting and receiving digital data signals from an isolated power domain to a local system power domain with up to 5 kV of isolation. Each part has four unidirectional digital isolation channels. In addition, Si88xx products include an integrated controller and switches for a dc-dc converter which regulates output voltage by sensing it on the isolated side.

2.2. Digital Isolation

The operation of an Si88xx digital channel is analogous to that of a digital buffer, except an RF carrier transmits data across the isolation barrier. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si88xx channel is shown in Figure 6.

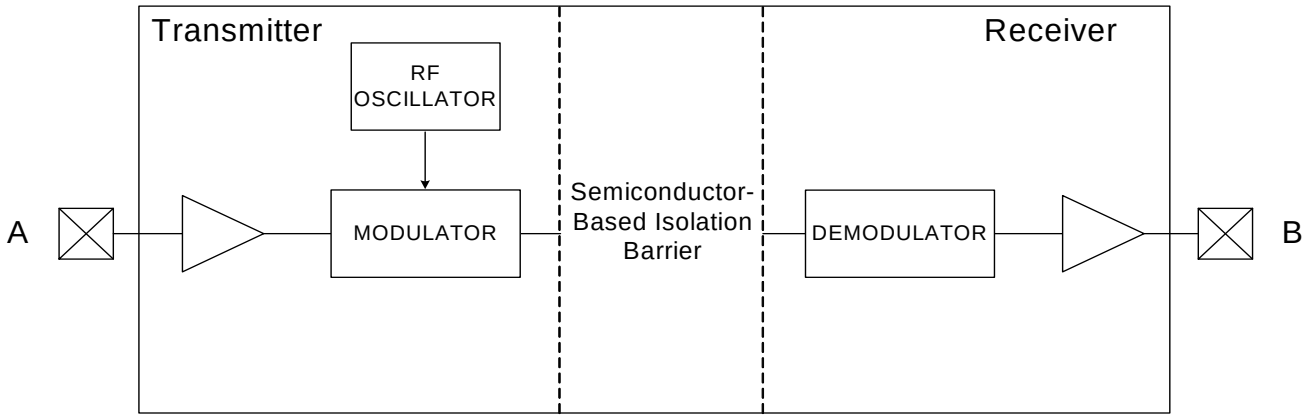


Figure 6. Simplified Si88xx Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a silicon dioxide capacitive isolation barrier. In the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 7 for more details.

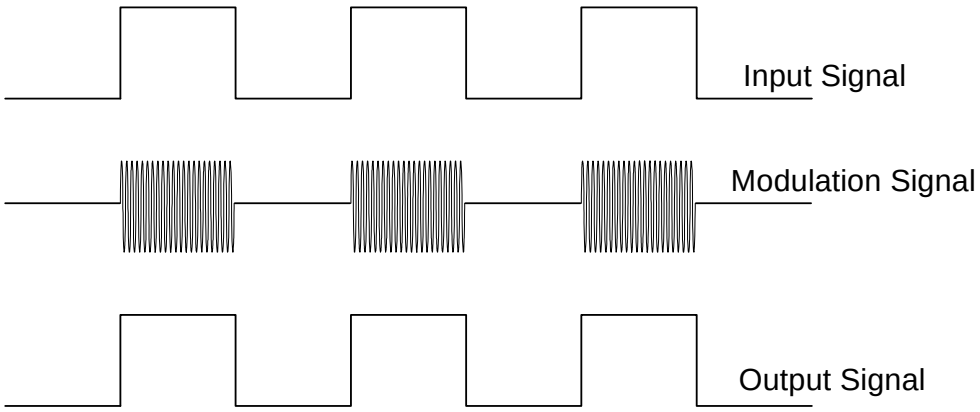


Figure 7. Modulation Scheme

2.3. DC-DC Converter Application Information

The Si88xx isolated dc-dc converter is based on a modified fly-back topology and uses an external transformer and Schottky rectifying diode for low cost and high operating efficiency. The PWM controller operates in closed-loop, peak current mode control and generates isolated output voltages with 2 W average output power at 5.0 V. Options are available for 24 Vdc input or output operation and externally configured switching frequency.

The dc-dc controller modulates a pair of internal primary-side power switches (see Figure 8) to generate an isolated voltage at external diode D1 cathode. Closed-loop feedback is provided by a compensated error amplifier, which compares the voltage at the VSNS pin to an internal voltage reference. The resulting error voltage is fed back through the isolation barrier via an internal feedback path to the controller, thus completing the control loop.

For higher input supply voltages than 5 V, an external FET Q2 is modulated by a driver pin ESW as shown in (see Figure 9). A shunt resistor based voltage sense pin RSN provides current sensing capability to the controller.

Additional features include an externally-triggered shutdown of the converter functionality using the SH pin and a programmable soft start configured by a capacitor connected to the SS pin. The Si88xx can be used in low- or high-voltage configurations. These features and configurations are explained in more detail below.

2.3.1. Shutdown

This feature allows the operation of the dc-dc converter to be shut down when asserted high. This function is provided by pin 6 (labeled “SH” on the Si882xx) and pin 7 (labeled “SH_FC” on the Si883xx and Si886xx). This feature is not available on the Si884xx. Pin 6 or pin 7 provide the exact same functionality and shut down the dc-dc converter when asserted high. For normal operation, pins 6 and 7 should be connected to ground.

2.3.2. Soft-Start

The dc-dc controller has an internal timer that controls the power conversion start-up to limit inrush current. There is also the Soft Start option where users can program the soft start up by an external capacitor connected to the SS pin. This feature is available on the Si883xx and the Si886xx.

2.3.3. Programmable Frequency

The frequency of the PWM modulator is set to a default of 250 kHz for Si882xx/4xx. Users can program their desired frequency within a given band of 200 kHz to 800 kHz by controlling the time constant of an external RC connected to the SH_FC and SS pins for Si883xx/6xx.

2.3.4. External Transformer Driver

The dc-dc controller has internal switches (VSW) for driving the transformer with up-to a 5.5 V voltage supply. For higher voltages on the primary side, a driver output (ESW) is provided that can drive an external NMOS power transistor for driving the transformer. When this configuration is used, a shunt resistor based voltage sense pin (RSN) provides current sensing to the controller.

2.3.5. VREGA, VREGB

For supporting voltages greater than 5.5 V, an internal voltage regulator (VREGA, VREGB) needs to be used in conjunction with an external NPN transistor, a resistor and a capacitor to provide regulated voltage to the IC.

2.3.6. Output Voltage Control

The isolated output voltage (VOUT) is sensed by a resistor divider that provides feedback to the controller through the VSNS pin. The voltage error is encoded and transmitted back to the primary side controller across the isolation barrier, which in turn changes the duty cycle of the transformer driver. The equation for VOUT is as follows:

$$VOUT = VSNS \times \left(1 + \frac{R1}{R2}\right) + R1 \times I_{OFFSET}$$

2.3.7. Compensation

The dc-dc converter uses peak current mode control. The loop is compensated by connecting an external resistor in series with a capacitor from the COMP pin to GNDB. The compensation resistance, RCOMP is fixed at 49.9 kΩ for Si882xx/3xx and 100 kΩ for Si884xx/6xx to match internal resistance. Capacitance value is given by the following equation, where f_C is crossover frequency:

$$CCOMP = \frac{6}{(2 \times \pi \times f_C \times RCOMP)}$$

For more details on the calculations involved, please see “AN892: Design Guide for Isolated DC/DC Using the Si882xx/883xx”.

2.3.8. Thermal Protection

A thermal shutdown circuit is included to protect the system from over-temperature events. The thermal shutdown is activated at a junction temperature that prevents permanent damage from occurring.

2.3.9. Cycle Skipping

Cycle skipping is included to reduce switching power losses at light loads. This feature is transparent to the user and is activated automatically at light loads. The product options with integrated power switches (Si882xx/3xx) may never experience cycle skipping during operation even at light loads while the external power switch options (Si884xx/6xx) are likely to have cycle skipping start at light loads.

2.3.10. Low-Voltage Configuration

The low-voltage configuration is used for converting 3.0 V to 5.5 V. All product options of the Si882xx and Si883xx are intended for this configuration.

An advantage of Si88xx devices over other converters that use this same topology is that the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation while reducing external components and increasing lifetime reliability.

In a typical digital signal isolation application, the dc-dc powers the Si882xx and Si883xx VDDB as shown in Figure 8. In addition to powering the isolated side of the dc-dc can deliver up to 2 W of power to other loads. The dc-dc requires an input capacitor, C2, blocking capacitor, C1, transformer, T1, rectifying diode, D1, and an output capacitor, C3. Resistors R1 and R2 divide the output voltage to match the internal reference of the error amplifier. Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. Though it is not necessary for normal operation, we recommend that a snubber be used to minimize radiated emissions. More details can be found in “AN892: Design Guide for Isolated DC-DC Using the Si882xx/883xx”.

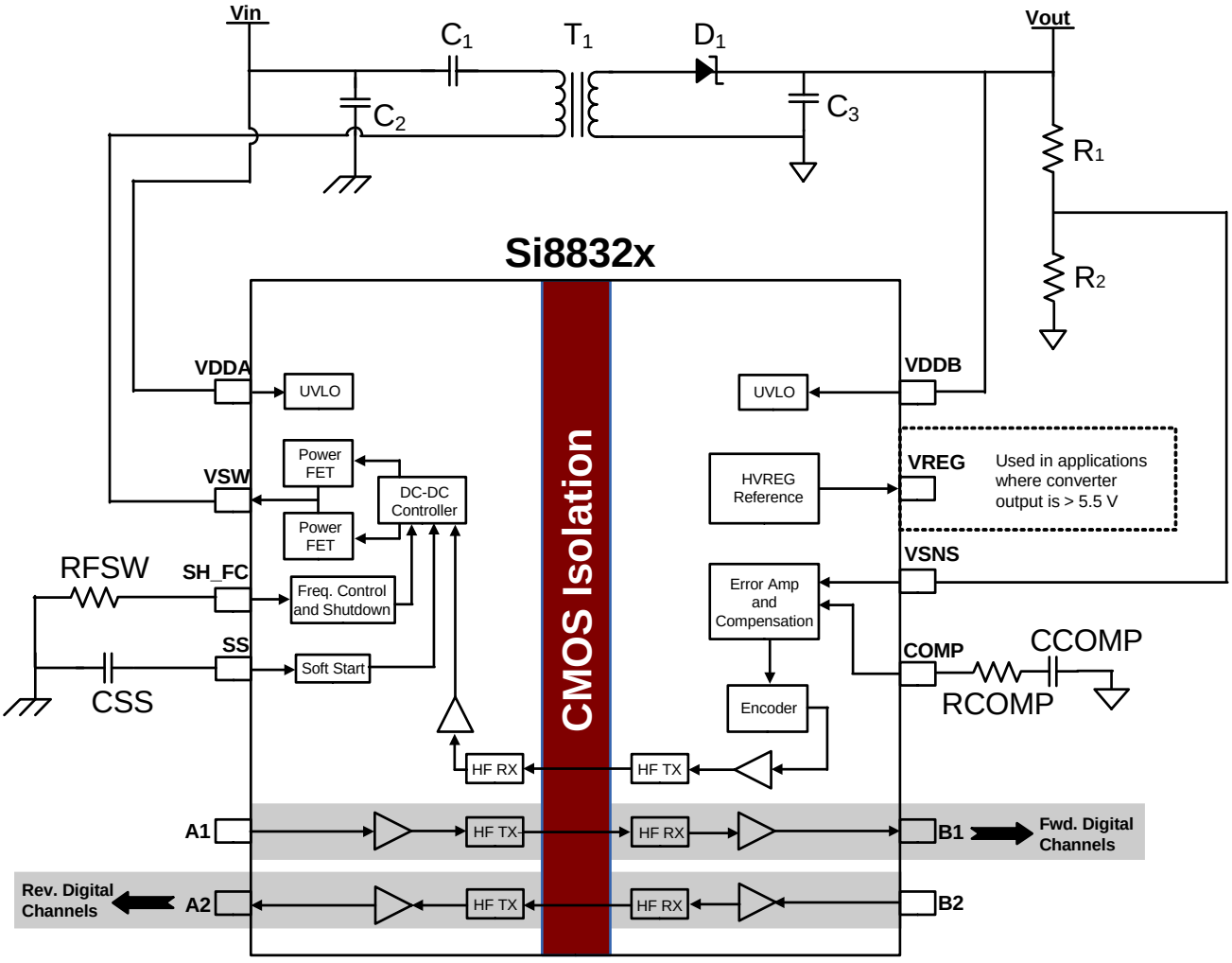


Figure 8. Si88xx Block Diagram: 3 V–5 V Input to 3 V–5 V Output

2.3.11. High-Voltage Configuration

The high-voltage configuration is used for converting up to 24 V to 3.3 V or 5.0 V. All product options of the Si884xx and Si886xx are intended for this configuration.

Si884xx and Si886xx can be used for dc-dc applications that have primary side voltage greater than 5.5 V. The dc-dc converter uses the isolated flyback topology. With this topology, the switch and sense resistor are external, allowing higher switching voltages. Digital isolator supply VDDA of the Si884xx and Si886xx require a supply less than or equal to 5.5 V. If a suitable supply is not available on the primary side, the VREGA voltage reference with external NPN transistor can supply VDDA. This eliminates the need to design an additional linear regulator circuit. Like the Si882xx and Si883xx, the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation.

Figure 9 shows the block diagram of an Si886xx with external components. Si886xx is different from the Si882xx/883xx as it has externally-controlled switching frequency and soft start. The dc-dc requires input capacitor C2, transformer T1, switch Q1, sense resistor R4, rectifying diode D1 and an output capacitor C3. To supply VDDA, Q2 transistor is biased and filtered by R3 and C1. External frequency and soft start behavior is set by CSS and RFSW. Resistors R1 and R2 divide the output voltage to match the internal reference of the error amplifier. Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. Though it is not necessary for normal operation, we recommend to use a snubber, to minimize high-frequency emissions. For further details, see "AN901: Design Guide for Isolated DC-DC Using the Si884xx/886xx".

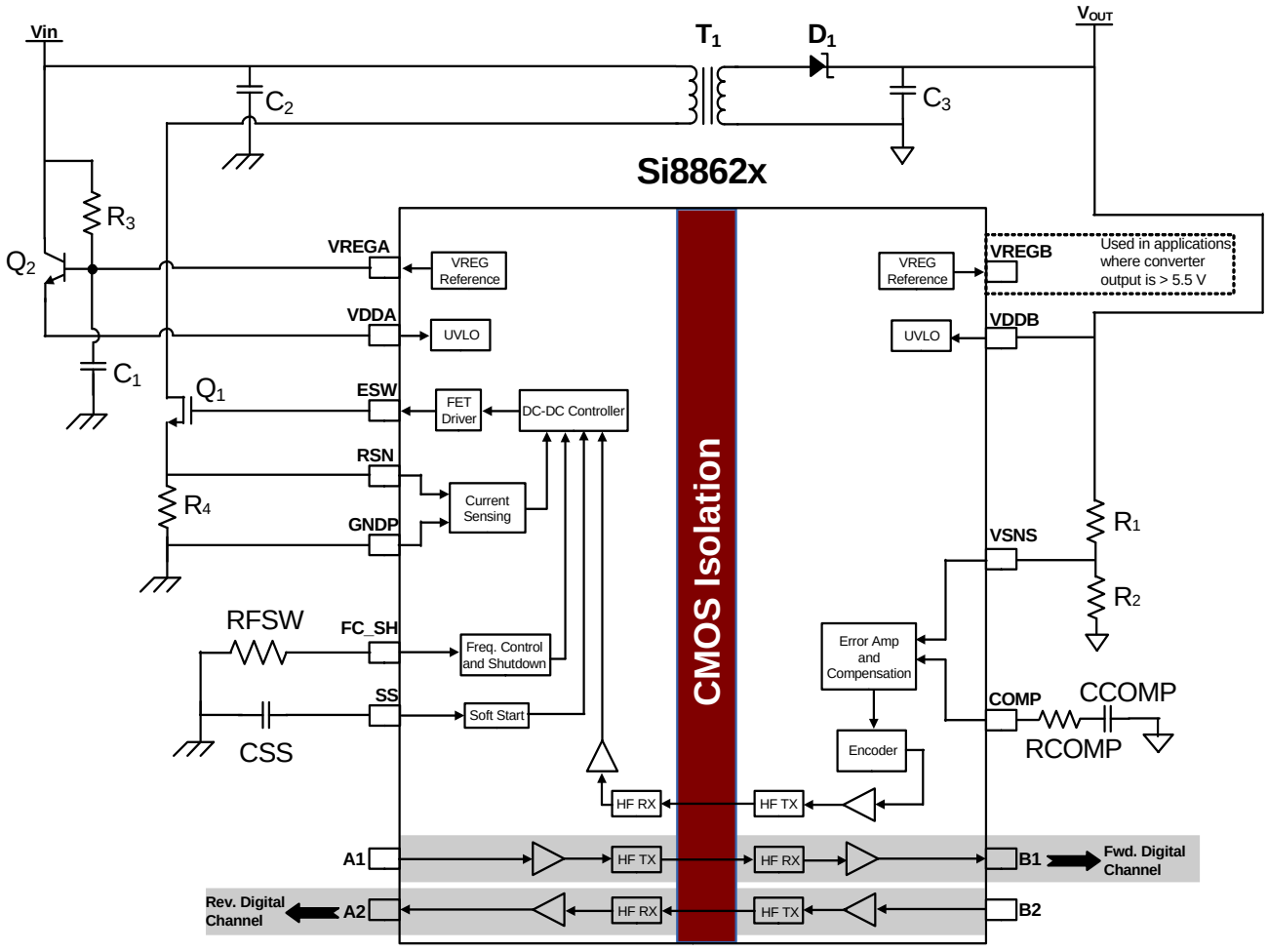


Figure 9. Si88xx Block Diagram: 24 V Input to 5 V Output

2.4. Transformer Design

Table 10 provides a list of transformers and their parametric characteristics that have been validated to work with Si882xx/3xx products (input voltage of 3 to 5 V) and Si884xx/Si886xx products (input voltage of 24 V). It is recommended that users order the transformers from the vendors per the part numbers given below. Refer to AN892 and AN901 for voltage translation applications not listed below.

To manufacture transformers from your preferred suppliers that may not be listed below, please specify to supplier the parametric characteristics as specified in the table below for a given input voltage and isolation rating.

Table 10. Transformer Specifications

Transformer Supplier	Ordering Part #	Input Voltage	Turns Ratio	Leakage Inductance	Primary Inductance	Primary Resistance	Isolation Rating
UMEC www.umec-usa.com	TG-UTB02185s	3.0 – 5.5 V	4.0:1	105 nH max	2 µH ± 5%	0.05 Ω max	2.5 kVrms
	TG-UTB02205s	24 V	3.0:1	800 nH max	25 µH ± 5%	0.135 Ω max	2.5 kVrms
Coilcraft www.coilcraft.com	TA7608-AL	3.0 – 5.5 V	4.0:1	60 nH max	2 µH ± 10%	0.036 Ω max	2.5 kVrms

3. Digital Isolator Device Operation

Table 11. Si88xx Logic Operation

VI Input	VDDI[1,2,3,4]	VDDO[1,2,3,4]	VO Output	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L[4] H[4]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I.

Notes:
1. VDDI and VDDO are the input and output power supplies. VI and VO are the respective input and output terminals.
2. P = powered; UP = unpowered.
3. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current. This situation should be avoided. We recommend that I/O's not be driven high when primary side supply is turned off or when in dc-dc shutdown mode.
4. See "5. Ordering Guide" on page 38 for details. This is the selectable fail-safe operating mode (ordering option). When VDDB is powered via the primary side and the integrated dc-dc, the default outputs are undetermined as secondary side power is not available when primary side power shuts off.

3.1. Device Startup

Outputs are held low during power up until VDDx is above the UVLO threshold for time period t_{SU}. Following this, the outputs follow the states of inputs.

3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDx is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when VDDA falls below V_{DDUV-} and exits UVLO when VDDA rises above V_{DDUV+}. Side B operates the same as Side A with respect to its VDD supply.

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4 and Table 6 detail the working voltage and creepage/clearance capabilities of the Si88xx. These tables also detail the component standards (UL1577, VDE0884-10, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1. Supply Bypass

The Si88xx family requires a 0.1 µF bypass capacitor between all VDDx and their associated GNDx. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.3.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving high-impedance terminated PCB traces, output pins should be source-terminated to minimize reflections.

3.4. Fail-Safe Operating Mode

Si88xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 11 and Table 13 for more information.

3.5. Typical Performance Characteristics

The typical performance characteristics are for information only. Refer to Table 2 for specification limits. The data below is for all channels switching.

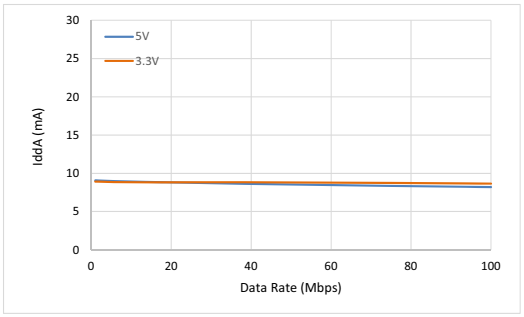


Figure 10. Si88240 Typical V_{DDA} Supply Current vs. Data Rate (5 and 3.3 V Operation)

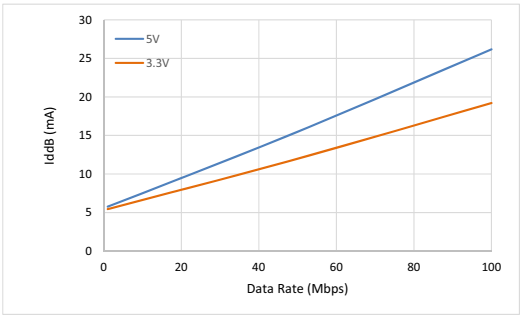


Figure 11. Si88240 Typical V_{DDB} Supply Current vs. Data Rate (5 and 3.3 V Operation)

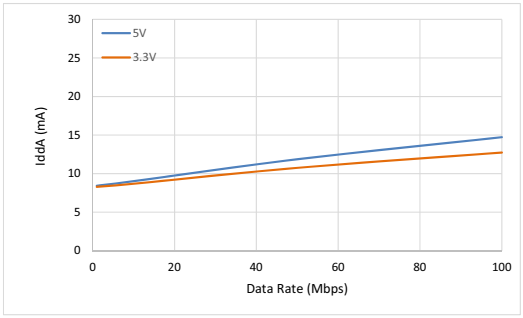


Figure 12. Si88241 Typical V_{DDA} Supply Current vs. Data Rate (5 and 3.3 V Operation)

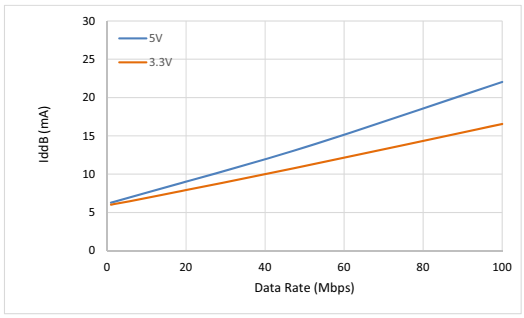


Figure 13. Si88241 Typical V_{DDB} Supply Current vs. Data Rate (5 and 3.3 V Operation)

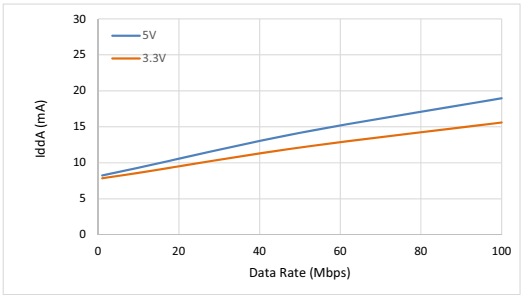


Figure 14. Si88242 Typical V_{DDA} Supply Current vs. Data Rate (5 and 3.3 V Operation)

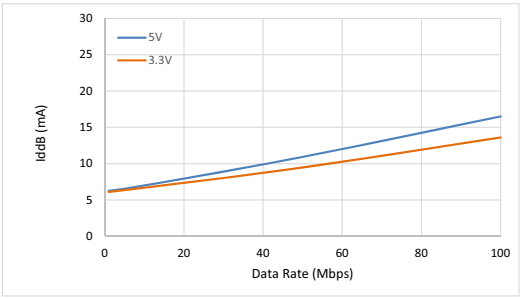


Figure 15. Si88242 Typical V_{DDB} Supply Current vs. Data Rate (5 and 3.3 V Operation)

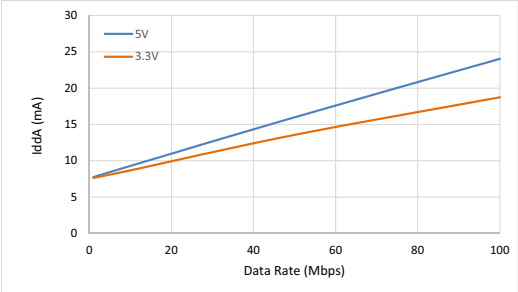


Figure 16. Si88243 Typical V_{DDA} Supply Current vs. Data Rate (5 and 3.3 V Operation)

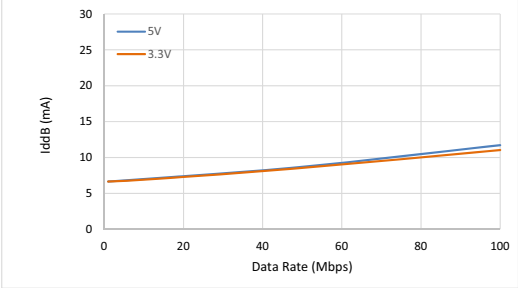


Figure 17. Si88243 Typical V_{DDB} Supply Current vs. Data Rate (5 and 3.3 V Operation)

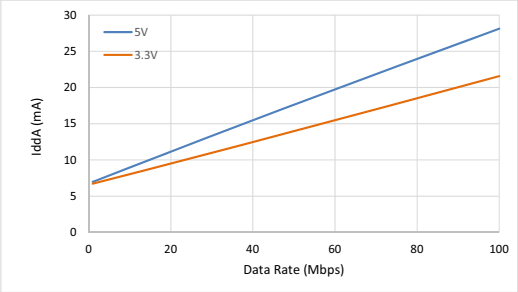


Figure 18. Si88244 Typical V_{DDA} Supply Current vs. Data Rate (5 and 3.3 V Operation)

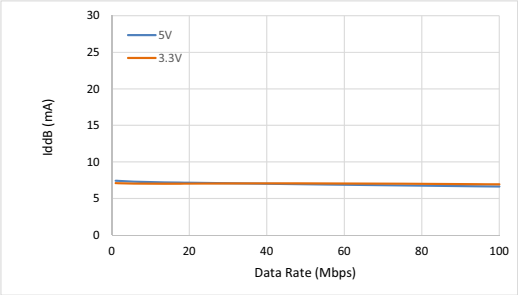


Figure 19. Si88244 Typical V_{DDB} Supply Current vs. Data Rate (5 and 3.3 V Operation)

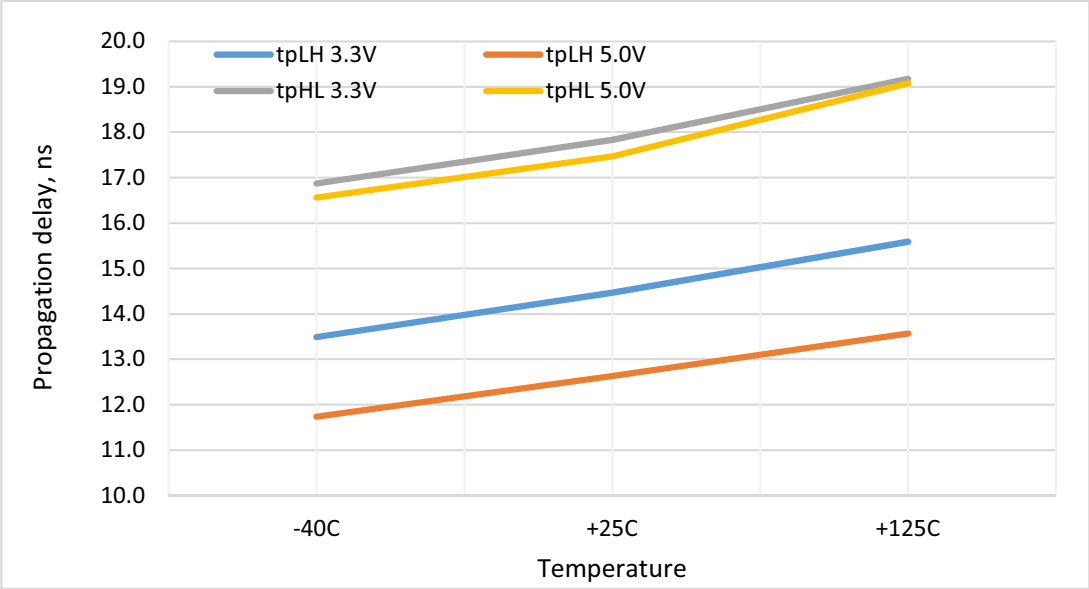


Figure 20. Propagation Delay vs. Temperature

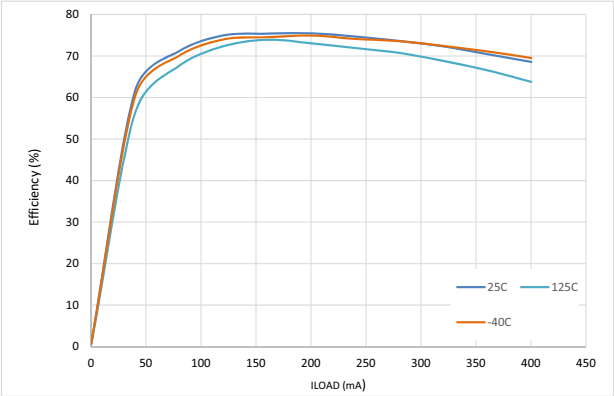


Figure 21. Efficiency vs. Load Current over Temperature (3.3 to 3.3 V)

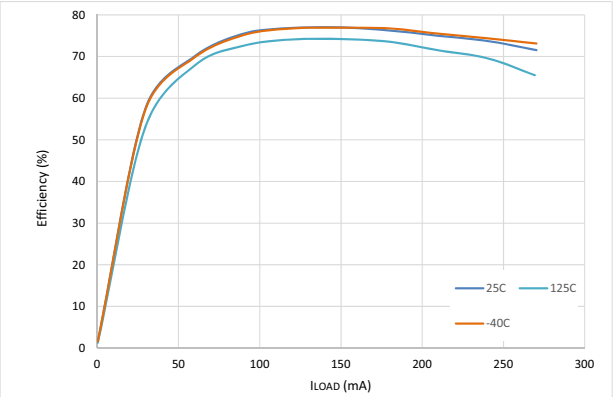


Figure 22. Efficiency vs. Load Current over Temperature (3.3 to 5.0 V)

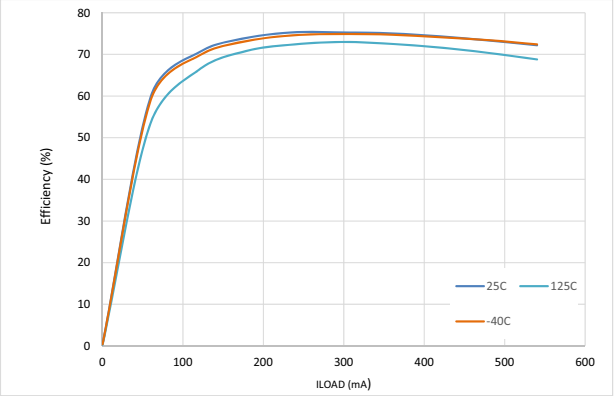


Figure 23. Efficiency vs. Load Current over Temperature (5.0 to 3.3 V)

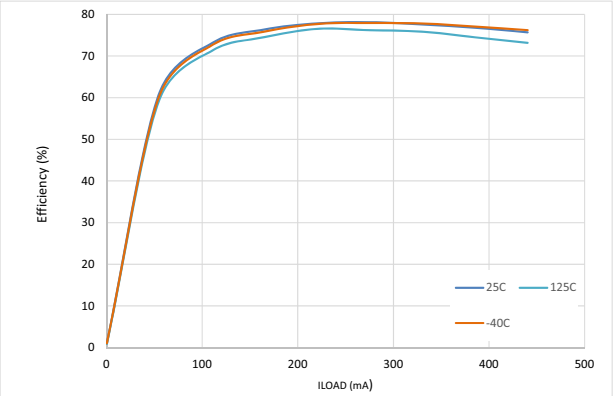


Figure 24. Efficiency vs. Load Current over Temperature (5.0 to 5.0 V)

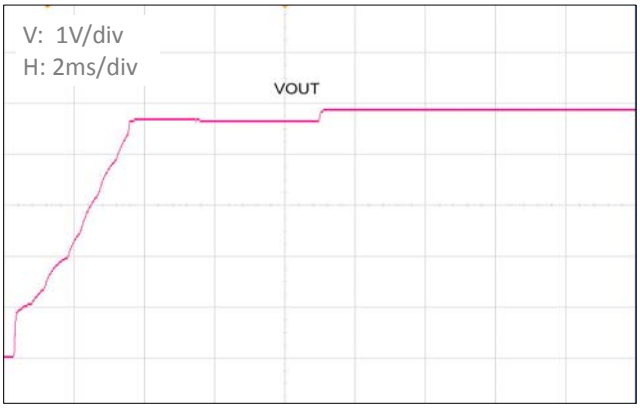


Figure 25. 5 V–5 V VOUT Startup vs.Time (No Load)

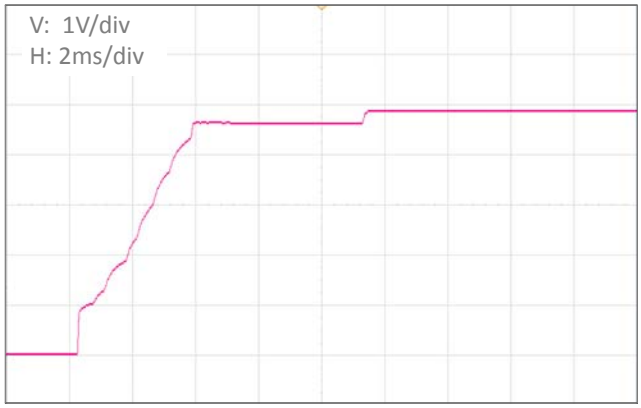


Figure 26. 5 V–5 V VOUT Startup vs.Time (10 mA Load Current)

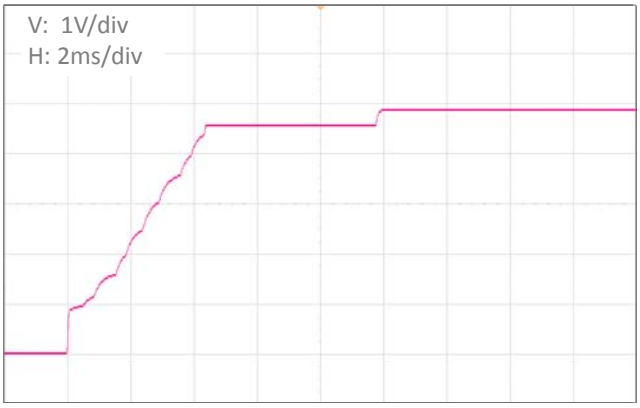


Figure 27. 5 V–5 V VOUT Startup vs.Time (50 mA Load Current)

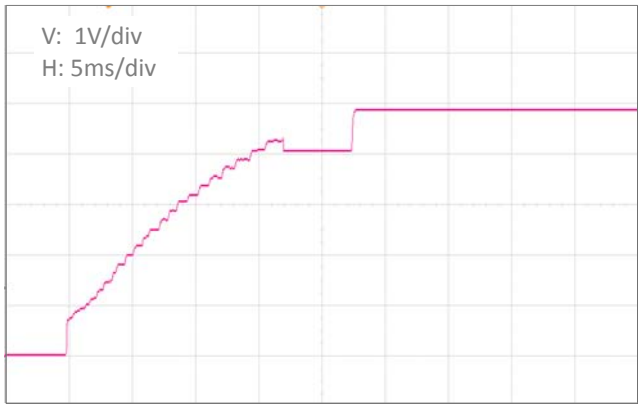


Figure 28. 5 V–5 V VOUT Startup vs.Time (400 mA Load Current)

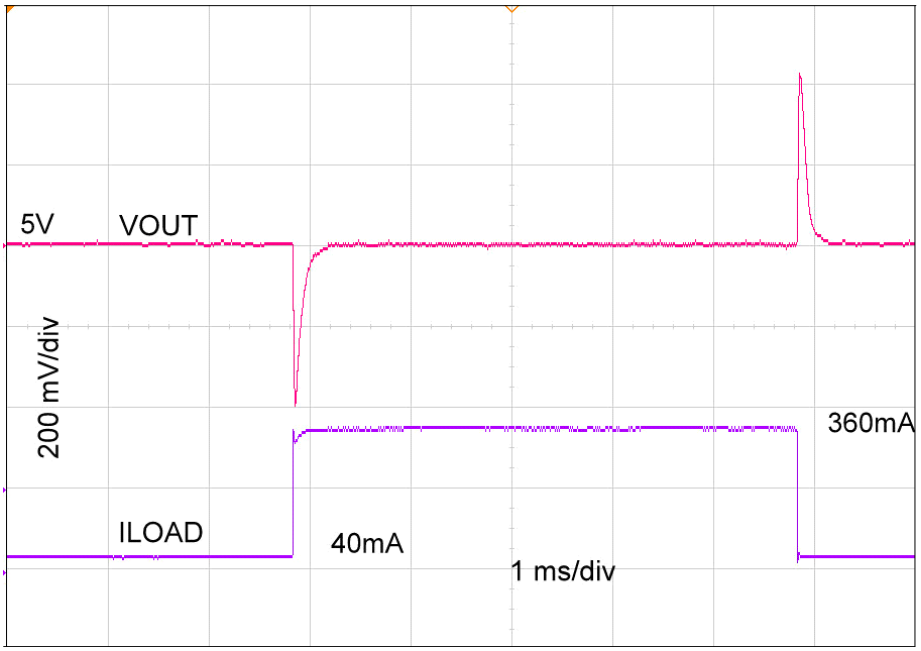


Figure 29. 5 V–5 V VOUT Load Transient Response, 10% to 90% Load

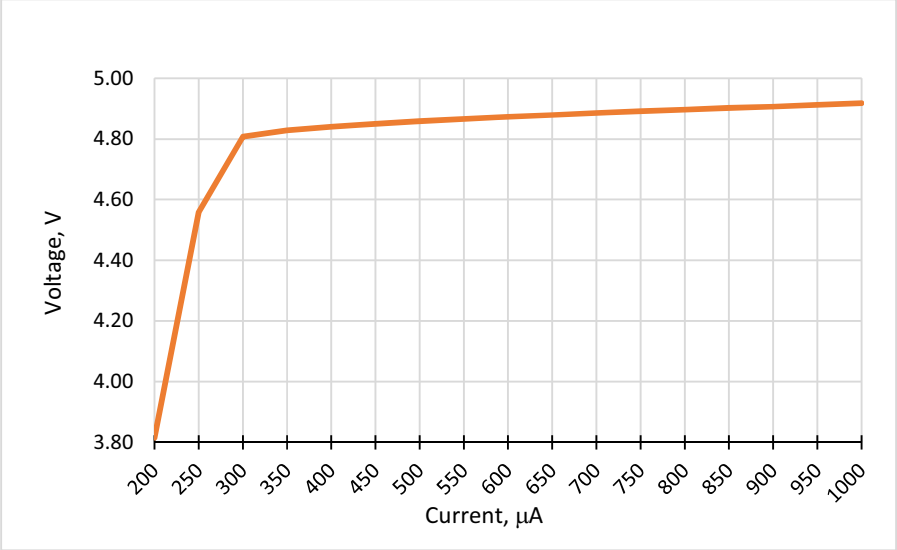


Figure 30. Typical I-V Curve for VREGA/B

4. Pin Descriptions

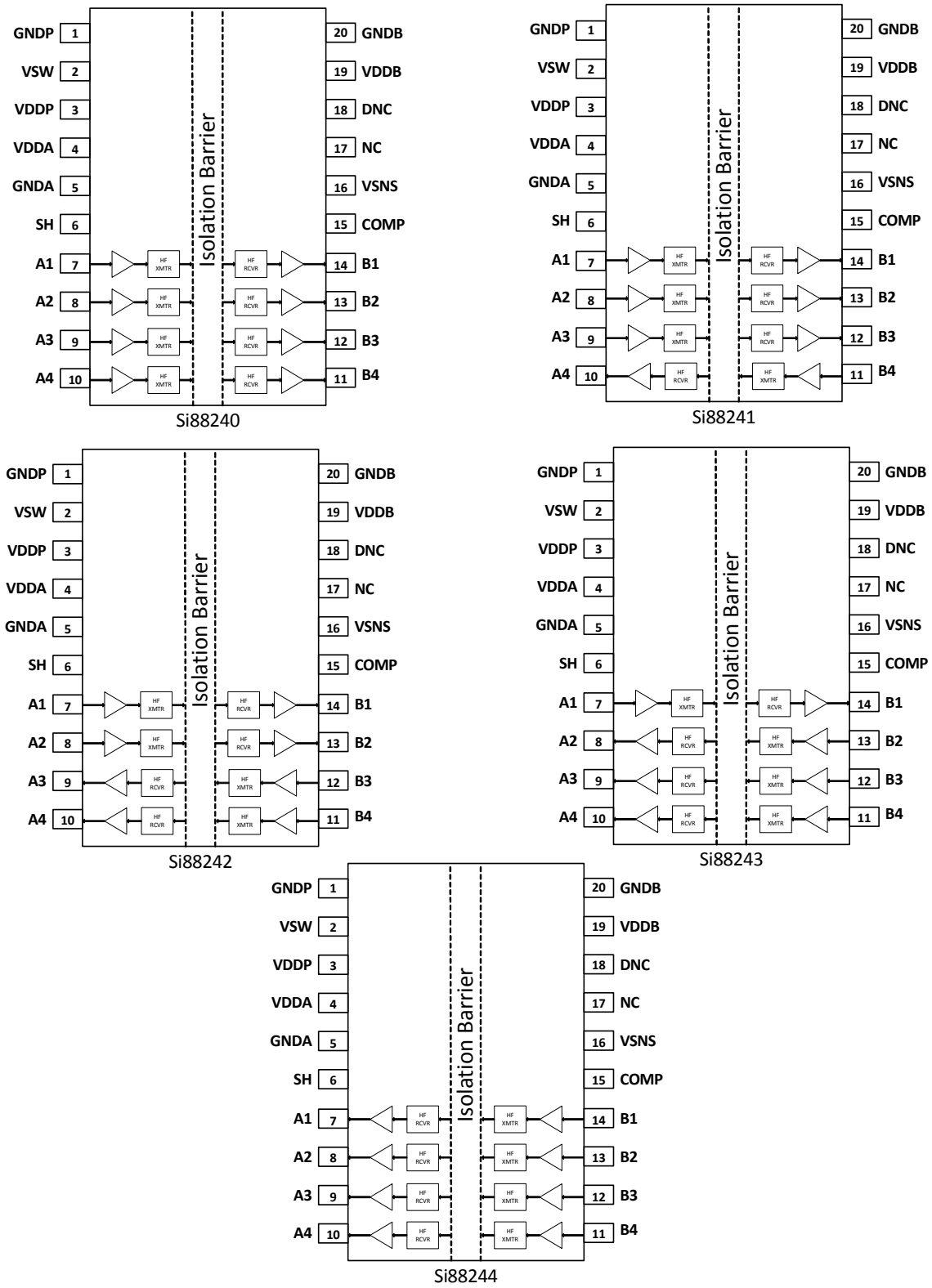


Figure 31. Si8824x Pin Configurations

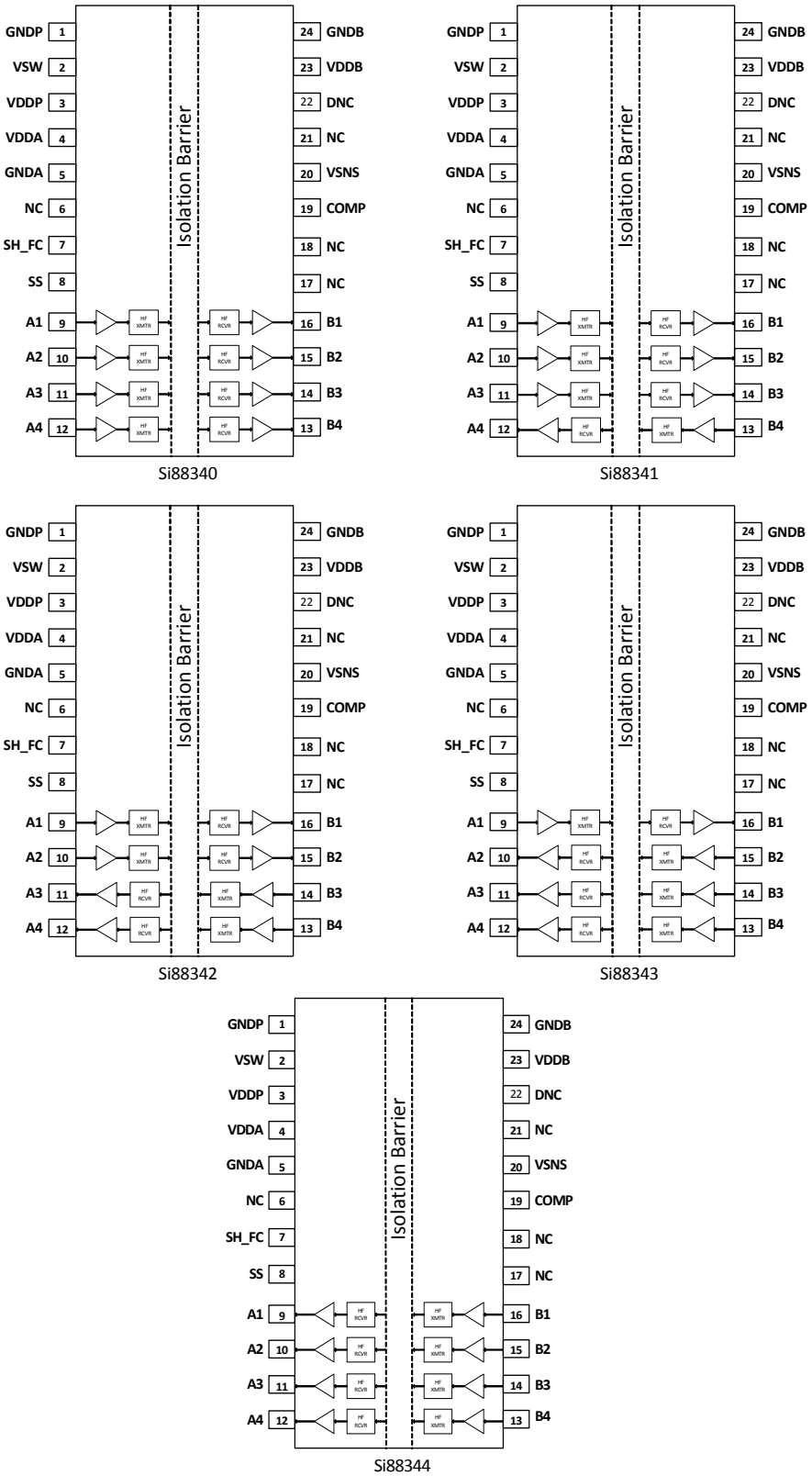


Figure 32. Si8834x Pinout Diagrams

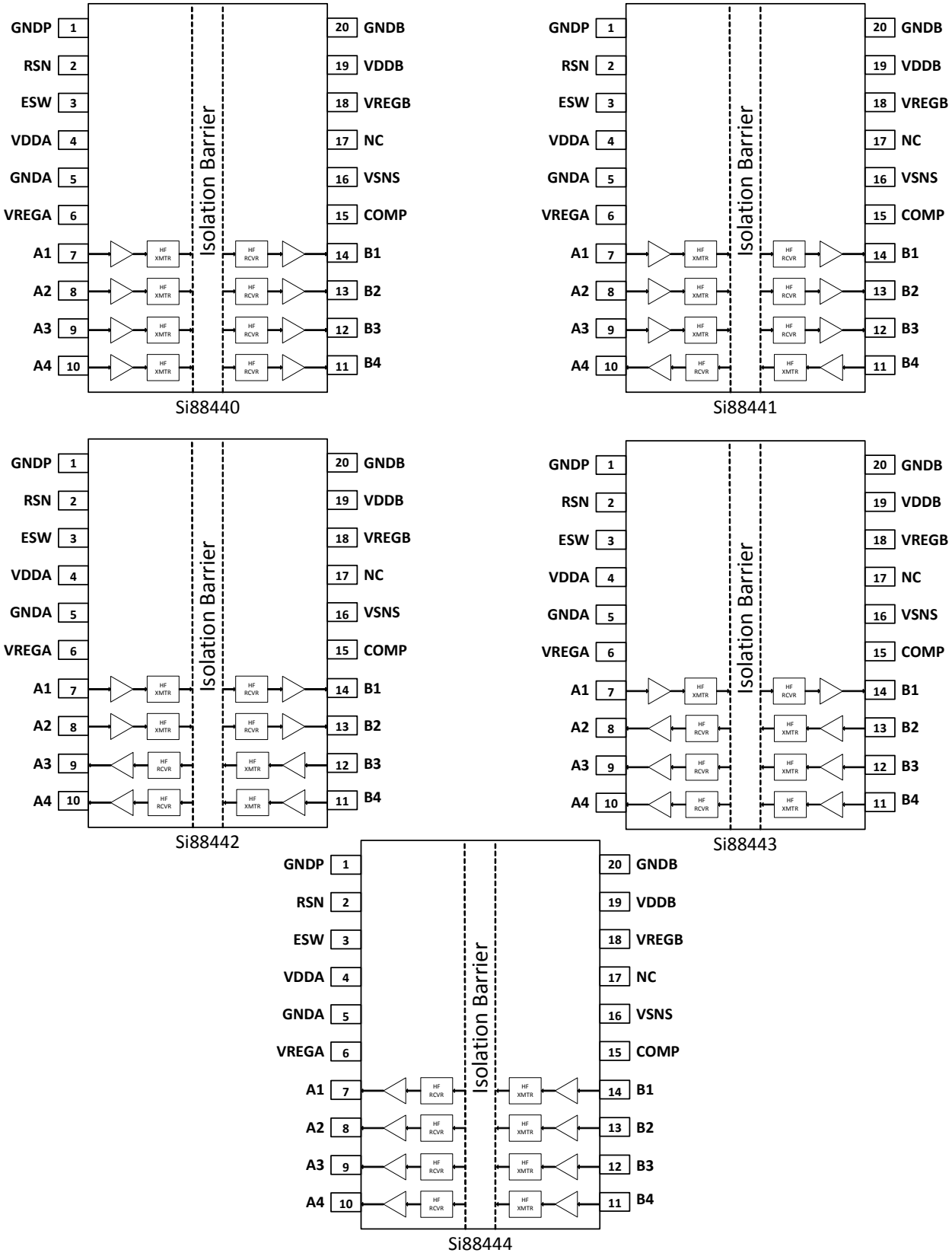


Figure 33. Si8844x Pinout Diagrams

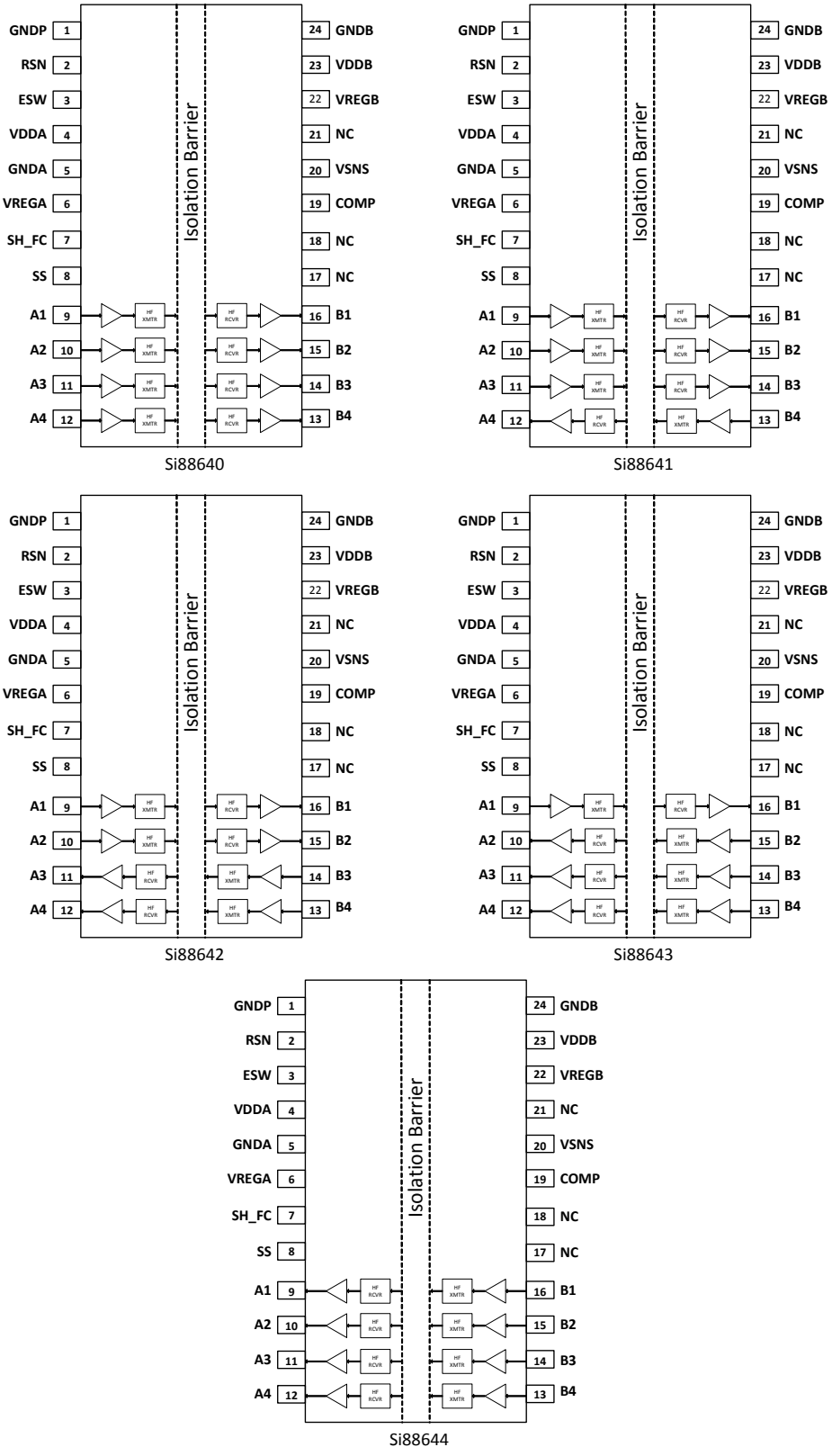


Figure 34. Si8864x Pinout Diagrams

Table 12. Si88x4x Pin Descriptions

Pin Name	Description
DC-DC Input Side	
VDDP	Power stage primary power supply.
VREGA	Voltage reference output for external voltage regulator pin.
GNDP	Power stage ground.
ESW	Power stage external switch driver output.
VSW	Power stage internal switch output.
SS	Soft startup control.
SH, SH_FC	Shutdown and Switch frequency control.
RSN	Power stage current sense input.
DC-DC Output Side	
VSNS	Power stage feedback input.
COMP	Power stage compensation.
VREGB	Voltage reference output for external voltage regulator pin.
DNC	Do not connect; leave open.
NC	No connect; this pin is not connected to the silicon.
Digital Isolator VDDA Side	
VDDA	Primary side signal power supply.
A1–A4	I/O signal channel 1–4.
GNDA	Primary side signal ground.
Digital Isolator VDDB Side	
VDDB	Secondary side signal power supply.
B1–B4	I/O signal channel 1–4.
GNDB	Secondary side signal ground.

5. Ordering Guide

Table 13. Si88x4x Ordering Guide[1,2,3,4]

Part #	DC-DC Shutdown	Soft Start Control	Frequency Control	External Switch	Forward Digital	Reverse Digital	Package
Product Options Available Now							
Si88240ED-IS	Y	N	N	N	4	0	WB SOIC-20
Si88241ED-IS	Y	N	N	N	3	1	WB SOIC-20
Si88242ED-IS	Y	N	N	N	2	2	WB SOIC-20
Si88243ED-IS	Y	N	N	N	1	3	WB SOIC-20
Si88244ED-IS	Y	N	N	N	0	4	WB SOIC-20
Contact Silicon Labs for Availability							
Si88240BD-IS	Y	N	N	N	4	0	WB SOIC-20
Si88241BD-IS	Y	N	N	N	3	1	WB SOIC-20
Si88242BD-IS	Y	N	N	N	2	2	WB SOIC-20
Si88243BD-IS	Y	N	N	N	1	3	WB SOIC-20
Si88244BD-IS	Y	N	N	N	0	4	WB SOIC-20
Si88340ED-IS	Y	Y	Y	N	4	0	WB SOIC-24
Si88341ED-IS	Y	Y	Y	N	3	1	WB SOIC-24
Si88342ED-IS	Y	Y	Y	N	2	2	WB SOIC-24
Si88343ED-IS	Y	Y	Y	N	1	3	WB SOIC-24
Si88344ED-IS	Y	Y	Y	N	0	4	WB SOIC-24
Si88440ED-IS	N	N	N	Y	4	0	WB SOIC-20
Si88441ED-IS	N	N	N	Y	3	1	WB SOIC-20
Si88442ED-IS	N	N	N	Y	2	2	WB SOIC-20
Si88443ED-IS	N	N	N	Y	1	3	WB SOIC-20
Si88444ED-IS	N	N	N	Y	0	4	WB SOIC-20
Si88640ED-IS	Y	Y	Y	Y	4	0	WB SOIC-24
Si88641ED-IS	Y	Y	Y	Y	3	1	WB SOIC-24
Si88642ED-IS	Y	Y	Y	Y	2	2	WB SOIC-24
Si88643ED-IS	Y	Y	Y	Y	1	3	WB SOIC-24
Si88644ED-IS	Y	Y	Y	Y	0	4	WB SOIC-24

Notes:

1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.
4. All Si88xxxEx product options are default output high on input power loss. All Si88xxxBx product options are default low. See "3. Digital Isolator Device Operation" on page 25 for more details about default output behavior.

6. Package Outline: 20-Pin Wide Body SOIC

Figure 35 illustrates the package details for the 20-pin wide-body SOIC package. Table 14 lists the values for the dimensions shown in the illustration.

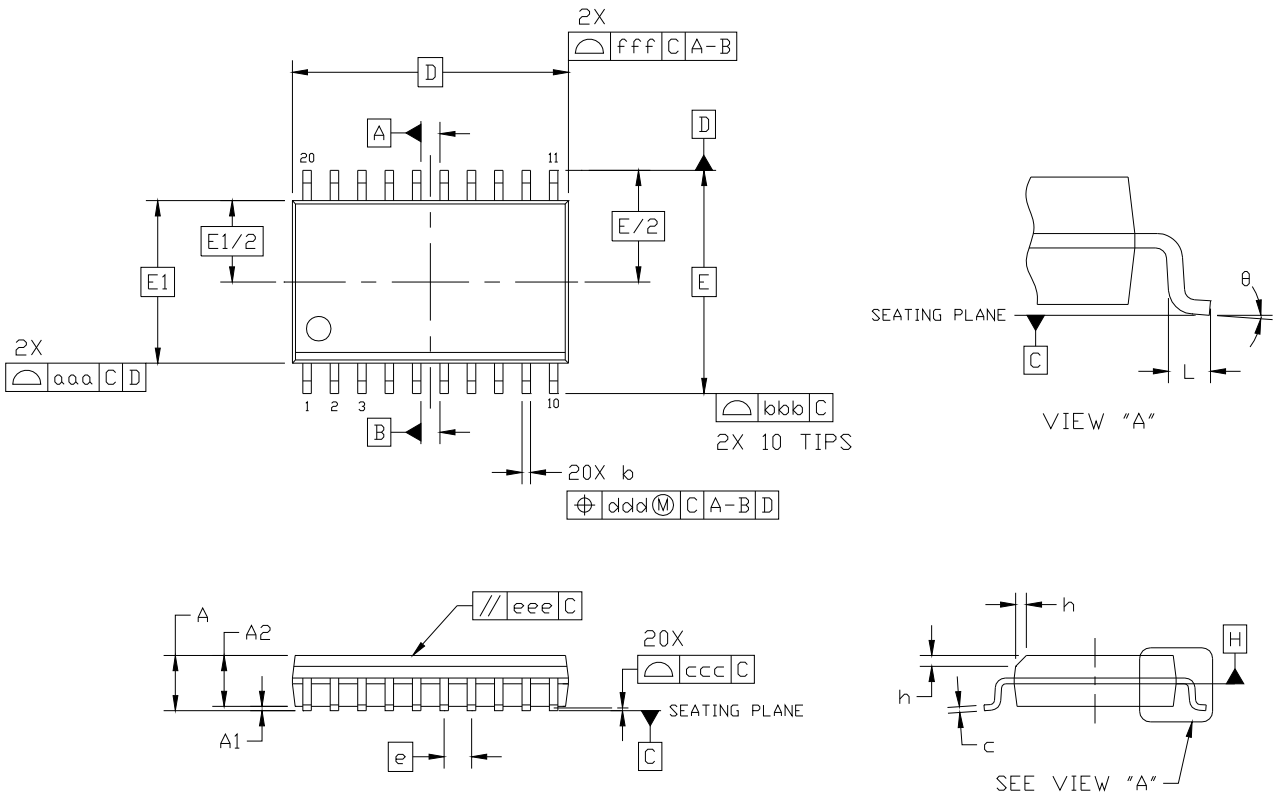


Figure 35. 20-Pin Wide Body SOIC

Table 14. 20-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	12.80 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AC.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

7. Land Pattern: 20-Pin SOIC

Figure 36 illustrates the PCB land pattern details for the 20-pin SOIC package. Table 15 lists the values for the dimensions shown in the illustration.

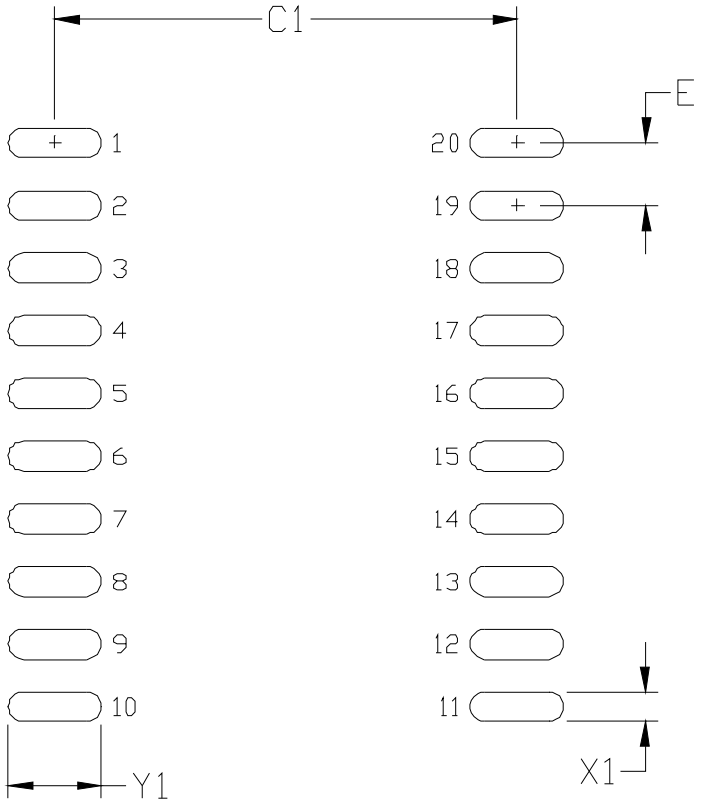


Figure 36. 20-Pin SOIC PCB Land Pattern

Table 15. 24-Pin SOIC PCB Land Pattern Dimensions

Dimension	mm
C1	9.40
E	1.27
X1	0.60
Y1	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline: 24-Pin Wide Body SOIC

Figure 37 illustrates the package details for the 24-pin wide-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

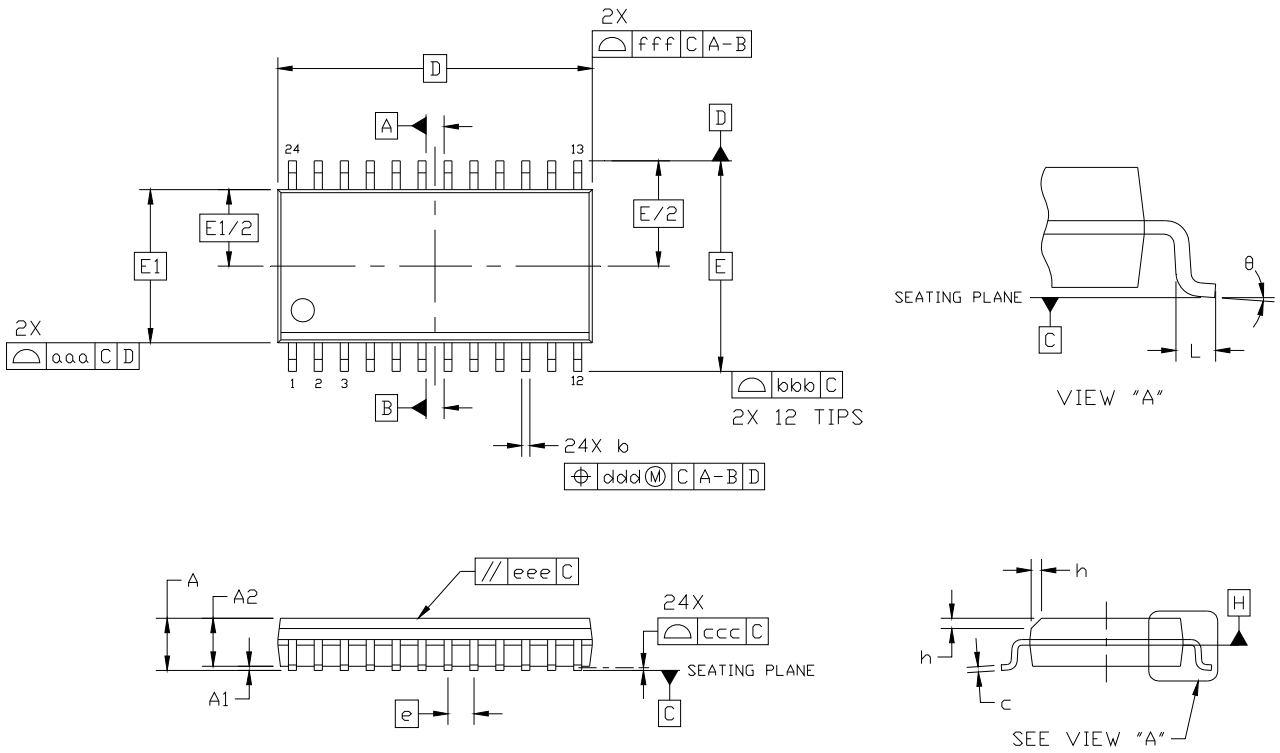


Figure 37. 24-Pin Wide Body SOIC

Table 16. 24-Pin Wide Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	15.40 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AD.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

9. Land Pattern: 24-Pin SOIC

Figure 38 illustrates the PCB land pattern details for the 24-pin SOIC package. Table 17 lists the values for the dimensions shown in the illustration.

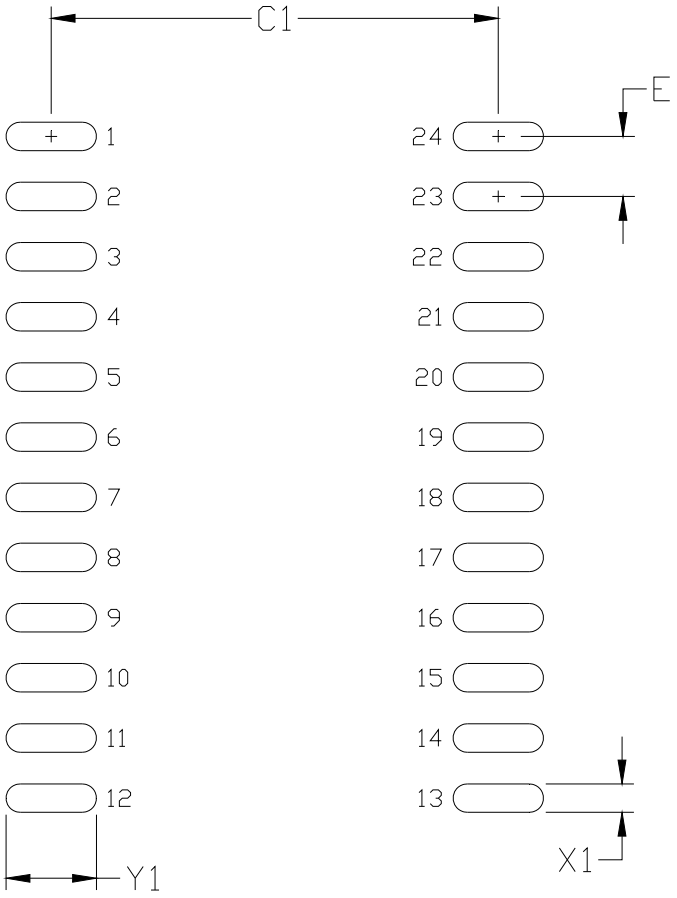


Figure 38. 24-Pin SOIC PCB Land Pattern

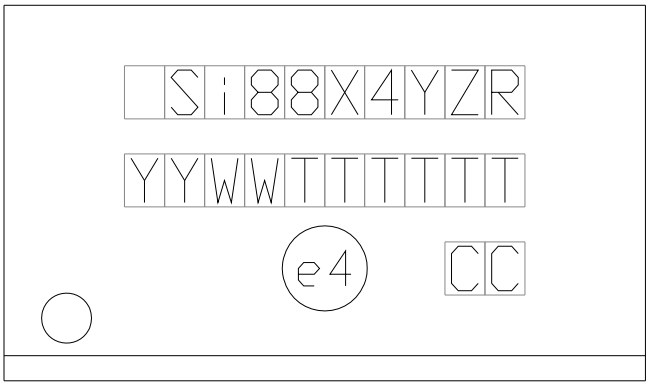
Table 17. 24-Pin SOIC PCB Land Pattern Dimensions

Dimension	mm
C1	9.40
E	1.27
X1	0.60
Y1	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Markings

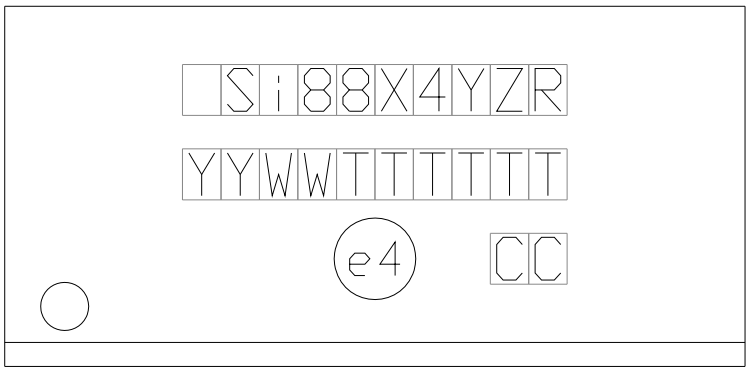
10.1. Si88x4x Top Marking (20-Pin Wide Body SOIC)



10.2. Top Marking Explanation (20-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si88x4 = 5 kV rated 4 channel digital isolator with dc-dc converter X = 2, 4 2 = dc-dc shutdown 4 = External FET Y = Number of reverse channels Z = E, B E = default high B = default low R = D D = 5 kVrms isolation rating
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

10.3. Si88x4x Top Marking (24-Pin Wide Body SOIC)



10.4. Top Marking Explanation (24-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si88x4 = 5kV rated 4 channel digital isolator with dc-dc converter X = 3, 6 3 = Full-featured dc-dc with internal FET 6 = Full-featured dc-dc with external FET Y = Number of reverse channels Z = E, B E = default high B = default low R = D D = 5 kVrms isolation rating
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 0.6

- Reformatted figures.
- Corrected typos.
- Added text for clarity.

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