

1:8 LOW JITTER CMOS CLOCK BUFFER WITH 2:1 INPUT MUX (<200 MHz)

Features

- 8 LVCMOS outputs
- Low additive jitter: 150 fs rms typ
- Wide-frequency range: dc to 200 MHz
- 2:1 input MUX
- Asynchronous output enable
- Low output-output skew: 40 ps typ
- RoHS compliant, Pb-free
- Industrial temperature range: -40 to +85 °C
- Footprint-compatible with ICS552-02
- 1.8, 2.5, or 3.3 V operation
- 16-TSSOP

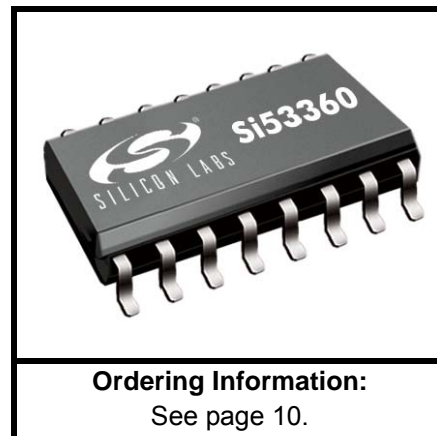
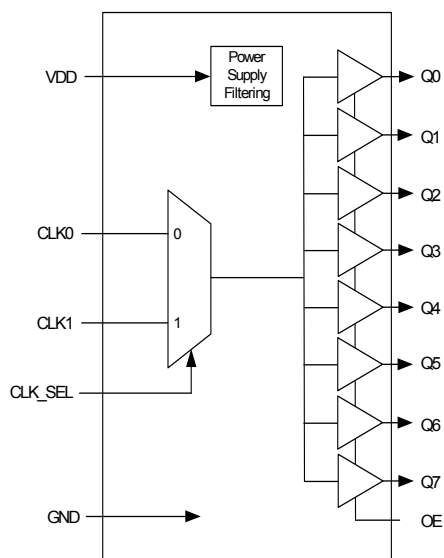
Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

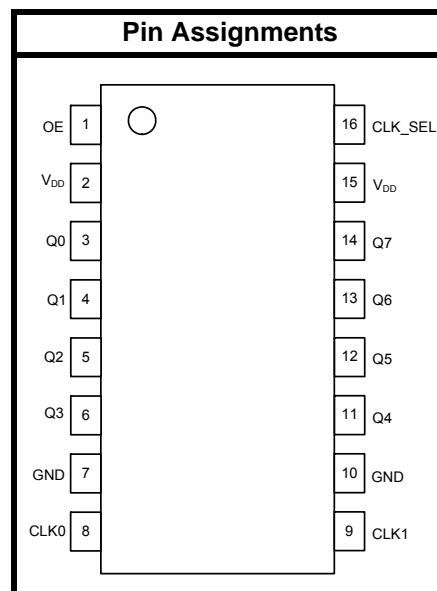
Description

The Si53360 is an ultra low jitter eight output LVCMOS buffer. The Si53360 features a 2:1 input mux, making it ideal for redundant clocking applications. The Si53360 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from dc to 200 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53360 supports operation over the industrial temperature range and can be operated from a 1.8 V, 2.5 V, or 3.3 V supply.

Functional Block Diagram



Ordering Information:
See page 10.



Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|----------|----------------|------|-----|------|------|
| Ambient Operating Temperature | T_A | | -40 | — | 85 | °C |
| Supply Voltage Range | V_{DD} | LVCMOS | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |

Table 2. Input Clock Specifications

($V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|---------------------|-----|---------------------|------|
| LVCMOS Input High Voltage | V_{IH} | $V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, $3.3\text{ V} \pm 10\%$ | $V_{DD} \times 0.7$ | — | — | V |
| LVCMOS Input Low Voltage | V_{IL} | $V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, $3.3\text{ V} \pm 10\%$ | — | — | $V_{DD} \times 0.3$ | V |
| Input Capacitance | C_{IN} | CLK0 and CLK1 pins with respect to GND | — | 5 | — | pF |

Table 3. DC Common Characteristics

($V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|----------------|---------------------|-----|---------------------|------------|
| Supply Current | I_{DD} | | — | 150 | — | mA |
| Input High Voltage | V_{IH} | CLK_SEL, OE | $0.8 \times V_{DD}$ | — | — | V |
| Input Low Voltage | V_{IL} | CLK_SEL, OE | — | — | $0.2 \times V_{DD}$ | V |
| Internal Pull-up Resistor | R_{UP} | OE, CLK_SEL | — | 25 | — | k Ω |

Table 4. Output Characteristics—LVCMOS

($V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------|----------|--|---------------------|-----|---------------------|------|
| Output Voltage High | V_{OH} | $I_{OH} = -12\text{ mA}$, $V_{DD} = 3.3\text{ V}$ $I_{OH} = -9\text{ mA}$, $V_{DD} = 2.5\text{ V}$ $I_{OH} = -6\text{ mA}$, $V_{DD} = 1.8\text{ V}$ | $0.8 \times V_{DD}$ | — | — | V |
| Output Voltage Low | V_{OL} | $I_{OL} = 12\text{ mA}$, $V_{DD} = 3.3\text{ V}$ $I_{OL} = 9\text{ mA}$, $V_{DD} = 2.5\text{ V}$ $I_{OL} = 6\text{ mA}$, $V_{DD} = 1.8\text{ V}$ | — | — | $0.2 \times V_{DD}$ | V |

Table 5. AC Characteristics

($V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------------|--|------|-----|-----|--------|
| Frequency | F | LVC MOS | dc | — | 200 | MHz |
| Duty Cycle Note: 50% input duty cycle. | D_C | 200 MHz, $50\ \Omega$ to $V_{DD}/2$, 20/80% $T_R/T_F < 10\%$ of period | 40 | 50 | 60 | % |
| Minimum Input Clock Slew Rate | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |
| Output Rise/Fall Time | T_R/T_F | 200 MHz, $50\ \Omega$, 20/80%, 2 pF load, 12 mA drive strength | — | — | 850 | ps |
| Minimum Input Pulse Width | T_W | | 2 | — | — | ns |
| Additive Jitter (12 kHz - 20 MHz) | J | 3.3 V, 200 MHz, $V_{in} = 1.7\text{ V}_{PP}$ @ 1 V/ns | — | 130 | 180 | fs-rms |
| | | 3.3 V, 156.25 MHz, $V_{in} = 2.18\text{ V}_{PP}$ @ 1 V/ns | — | 125 | 220 | fs-rms |
| | | 2.5 V, 200 MHz, $V_{in} = 1.7\text{ V}_{PP}$ @ 1 V/ns | — | 115 | 250 | fs-rms |
| | | 2.5 V, 156.25 MHz, $V_{in} = 2.18\text{ V}_{PP}$ @ 1 V/ns | — | 125 | 240 | fs-rms |
| Propagation Delay | T_{PLH} , T_{PHL} | Low-to-high, high-to-low Single-ended $C_L = 2\text{ pF}$ | 1.5 | 3.0 | 4.5 | ns |
| Output Enable Time | T_{EN} | F = 1 MHz | — | 10 | — | ns |
| | | F = 100 MHz | — | 10 | — | ns |
| Output Disable Time | T_{DIS} | F = 1 MHz | — | 20 | — | ns |
| | | F = 100 MHz | — | 20 | — | ns |
| Part to Part Skew | T_{SKPP} | $C_L = 2\text{ pF}$ | 0 | — | 300 | ps |
| Output to Output Skew | T_{SK} | $C_L = 2\text{ pF}$ | — | 20 | 80 | ps |

Table 6. Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---------------|----------------|-------|------|
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 124.4 | °C/W |

Table 7. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|------------|--|------|-----|----------------|------|
| Storage Temperature | T_S | | -55 | — | 150 | °C |
| Supply Voltage | V_{DD} | | -0.5 | — | 3.8 | V |
| Input Voltage | V_{IN} | | -0.5 | — | $V_{DD} + 0.3$ | V |
| Output Voltage | V_{OUT} | | — | — | $V_{DD} + 0.3$ | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 k Ω | — | — | 2000 | V |
| ESD Sensitivity | CDM | | — | — | 500 | V |
| Peak Soldering Reflow Temperature | T_{PEAK} | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | T_J | | — | — | 125 | °C |

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53360 is a low jitter, low skew 1:8 CMOS buffer with an integrated 2:1 input mux. A clock select pin is used to select the active input clock. An asynchronous output enable pin is available for additional control.

2.1. Input Termination

Figure 1 shows the recommended input clock termination.

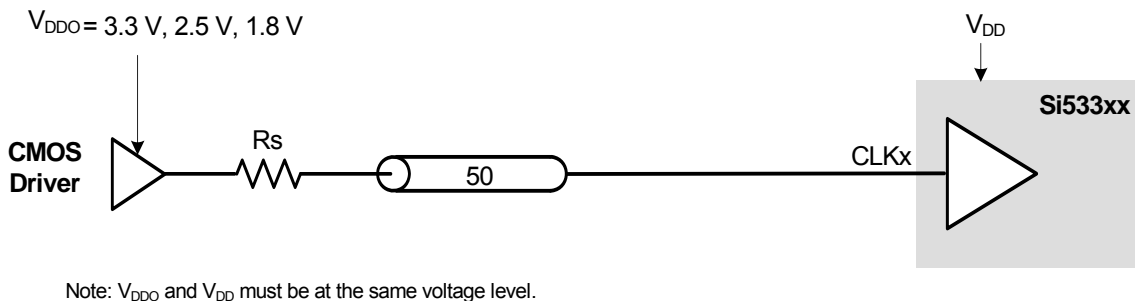


Figure 1. LVCMOS DC-Coupled Input Termination

2.2. Input Mux

The Si53360 provides two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings. If one of the input clocks is unused, leave floating.

Table 8. Input Mux and Output Enable Logic

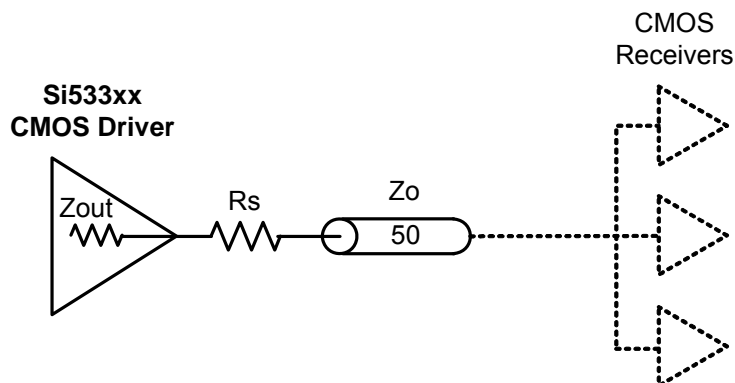
| CLK_SEL | CLK0 | CLK1 | OE ¹ | Q ² |
|---------|------|------|-----------------|----------------|
| L | L | X | H | L |
| L | H | X | H | H |
| H | X | L | H | L |
| H | X | H | H | H |
| X | X | X | L | Tri-state |

Notes:

1. Output enable active high.
2. On the next negative transition of CLK0 or CLK1.

2.3. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused output clocks should be left floating.



Note: $R_s = 33 \Omega$ for 3.3 V and 2.5 V operation.
 $R_s = 0 \Omega$ for 1.8 V operation.

Figure 2. LVCMOS Output Termination

2.4. AC Timing Waveforms

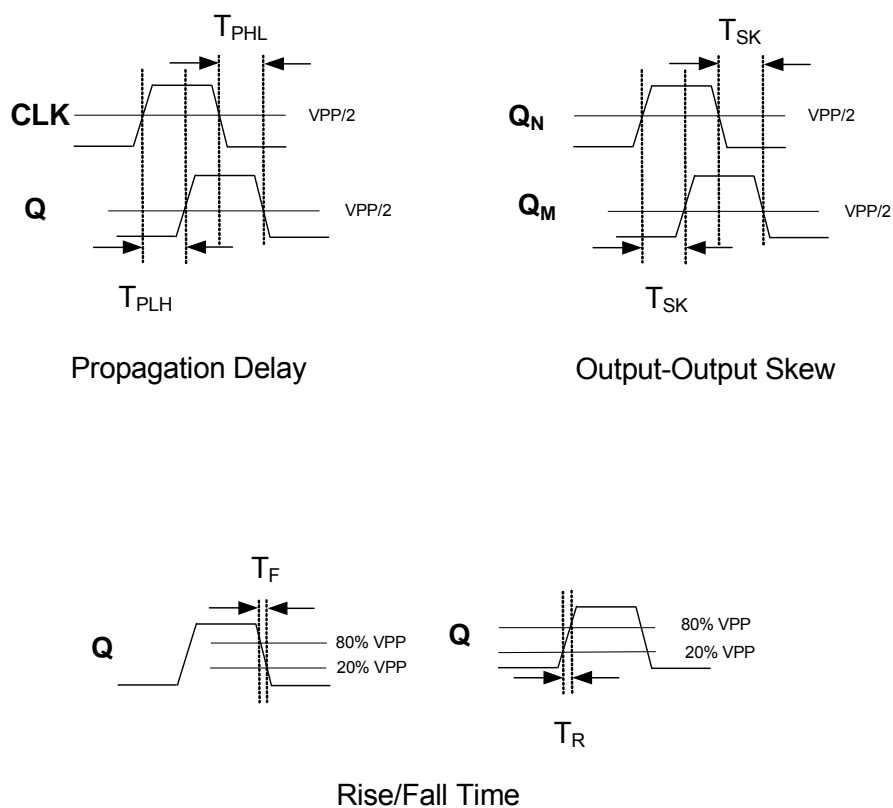


Figure 3. AC Waveforms

3. Pin Description: 16-TSSOP

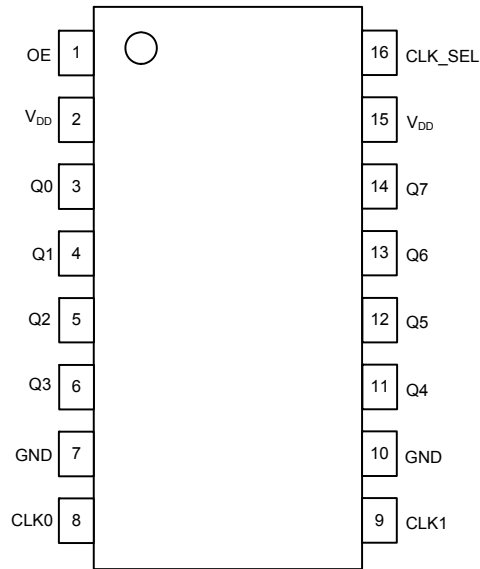


Table 9. Si53360 Pin Description*

| Pin # | Name | Type* | Description |
|-------|-----------------|-------|--|
| 1 | OE | I | Output enable. When OE= high, the clock outputs are enabled. When OE= low, the clock outputs are tri-stated. OE features an internal pull-up resistor, and may be left unconnected. |
| 2 | V _{DD} | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the V _{DD} pin as possible. |
| 3 | Q0 | O | Output clock 0. |
| 4 | Q1 | O | Output clock 1. |
| 5 | Q2 | O | Output clock 2. |
| 6 | Q3 | O | Output clock 3. |
| 7 | GND | GND | Ground. |
| 8 | CLK0 | I | Input clock 0. |
| 9 | CLK1 | I | Input clock 1. |
| 10 | GND | GND | Ground. |
| 11 | Q4 | O | Output clock 4. |
| 12 | Q5 | O | Output clock 5. |
| 13 | Q6 | O | Output clock 6. |
| 14 | Q7 | O | Output clock 7. |

*Note: Pin types are: I = input, O = output, P = power, GND = ground.

Table 9. Si53360 Pin Description* (Continued)

| Pin # | Name | Type* | Description |
|-------|-----------------|-------|---|
| 15 | V _{DD} | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the V _{DD} pin as possible. |
| 16 | CLK_SEL | I | Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL features an internal pull-up resistor. |

*Note: Pin types are: I = input, O = output, P = power, GND = ground.

Si53360

4. Ordering Guide

| Part Number | Package | PB-Free, ROHS-6 | Temperature |
|--------------|----------|-----------------|--------------|
| Si53360-B-GT | 16-TSSOP | Yes | -40 to 85 °C |

5. Package Outline

5.1. 16-TSSOP Package Diagram

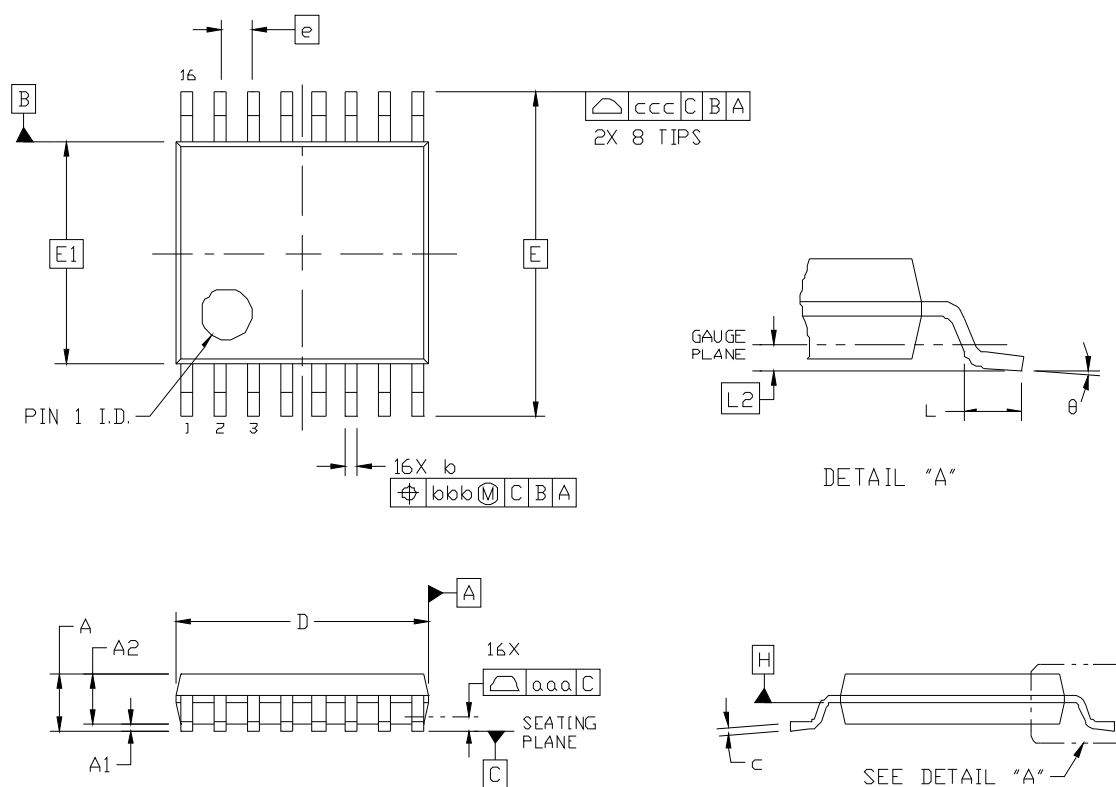


Figure 4. Si53360 16-TSSOP Package Diagram

Table 10. Package Dimensions

| Dimension | Min | Nom | Max | Dimension | Min | Nom | Max |
|-----------|----------|------|------|-----------|----------|------|------|
| A | — | — | 1.20 | e | 0.65 BSC | | |
| A1 | 0.05 | — | 0.15 | L | 0.45 | 0.60 | 0.75 |
| A2 | 0.80 | 1.00 | 1.05 | L2 | 0.25 BSC | | |
| b | 0.19 | — | 0.30 | θ | 0° | — | 8° |
| c | 0.09 | — | 0.20 | aaa | 0.10 | | |
| D | 4.90 | 5.00 | 5.10 | bbb | 0.10 | | |
| E | 6.40 BSC | | | ccc | 0.20 | | |
| E1 | 4.30 | 4.40 | 4.50 | | | | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. PCB Land Pattern

6.1. 16-TSSOP Package Land Pattern

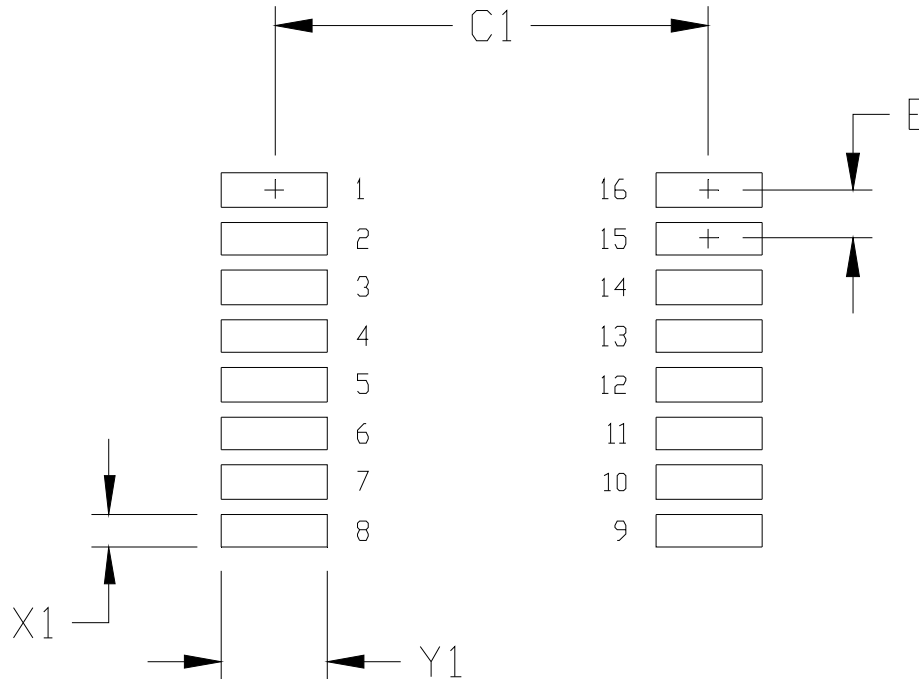


Figure 5. Si53360 16-TSSOP Package Land Pattern

Table 11. PCB Land Pattern

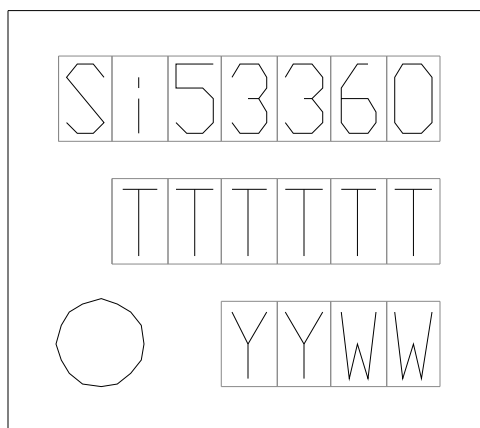
| Dimension | Feature | (mm) |
|-----------|--------------------|------|
| C1 | Pad Column Spacing | 5.80 |
| E | Pad Row Pitch | 0.65 |
| X1 | Pad Width | 0.45 |
| Y1 | Pad Length | 1.40 |

Notes:

1. This Land Pattern Design is based on IPC-7351 specifications for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7. Top Marking

7.1. Si53360 Top Marking



7.2. Top Marking Explanation

| | | |
|------------------------|--|--|
| Mark Method: | Laser | |
| Font Size: | 2.0 Point (0.71 mm) Right-Justified | |
| Line 1 Marking: | Customer Part Number | Si53360 |
| Line 2 Marking: | TTTTTT=Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking: | YY=Year WW=Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the build date. |

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 1.0

- Updated Table 2, “Input Clock Specifications,” on page 3.
- Updated Table 3, “DC Common Characteristics,” on page 3.
- Added Table 4, “Output Characteristics—LVCMOS,” on page 3.
- Updated Table 10, “Package Dimensions,” on page 11 to include improved data for additive jitter specifications.
- Updated output voltage specifications
- Improved performance specifications with more detail.
- Added pin type description to the pin descriptions table.

Revision 1.0 to Revision 1.1

- Updated Table 9, “Si53360 Pin Description*,” on page 8.



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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>