DUAL 1:5 LOW JITTER LVPECL CLOCK BUFFER (<1.25 GHZ)

Features

- 2 independant banks of LVPECL outputs
- Ultra-low additive jitter: 45 fs rms typ
- Wide frequency range: dc to 1.25 GHz
- Input compatible with LVPECL, LVDS, CML, HCSL, LVCMOS
- Low output-output skew: <25 ps typ
- RoHS compliant, Pb-free
- 32-QFN, 32-eLQFP
- Industrial temperature range: –40 to +85°C
- Footprint-compatible with MC100LVEP210

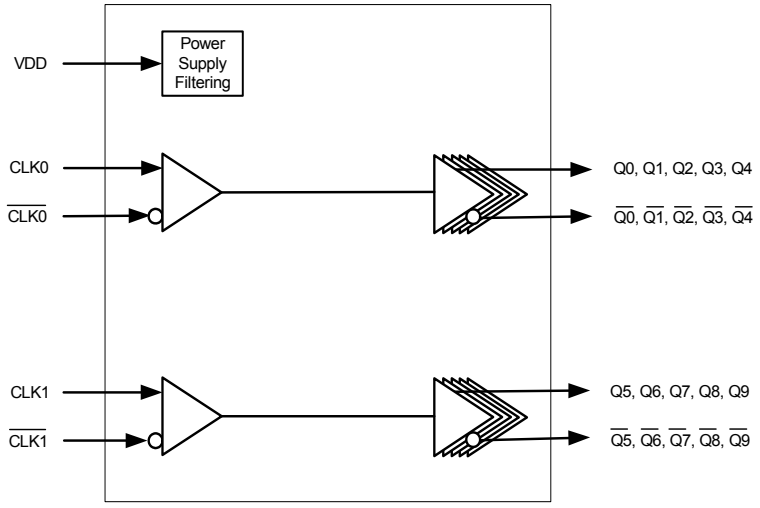
Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Description

The Si53325 is an ultra low jitter dual 1:5 LVPECL buffer. The Si53325 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from dc to 1.25 GHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53325 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments.

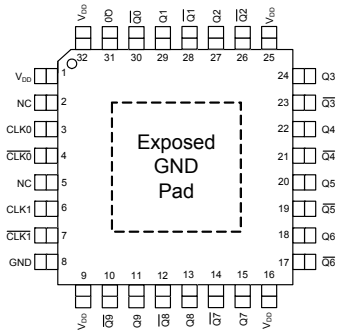
Functional Block Diagram

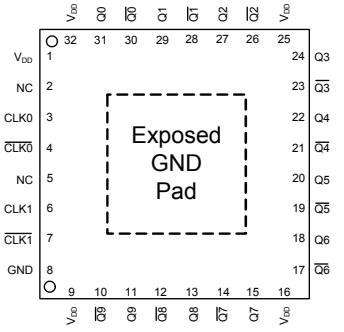


Ordering Information:
See page 18.

Pin Assignments

Si53325





Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range	V_{DD}	LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V

Table 2. Input Clock Specifications

(2.5 V ± 5%, or 3.3 V ± 10%, T_A=–40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	0.05	—	—	V
Differential Input Swing (peak-to-peak)	V_{IN}		0.2	—	2.2	V
LVCMOS Input High Voltage	V_{IH}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	V_{DD} x 0.7	—	—	V
LVCMOS Input Low Voltage	V_{IL}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	—	—	V_{DD} x 0.3	V
Input Capacitance	C_{IN}	CLK0 and CLK1 pins with respect to GND	—	5	—	pF

Table 3. DC Common Characteristics

(2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}	Measured using ac-coupled termination shown in Figure 6	—	440	—	mA

Table 4. Output Characteristics (LVPECL)

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	V_{COM}		V_{DD} – 1.595	—	V_{DD} – 1.245	V
Single-Ended Output Swing*	V_{SE}		0.40	0.80	1.050	V
***Note:** Unused outputs can be left floating. Do not short unused outputs to ground.						

Table 5. AC Characteristics

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F		dc	—	1250	MHz
Duty Cycle **Note:** 50% input duty cycle.	D_C	20/80% T_R/T_F<10% of period (Differential input clock)	47	50	53	%
Duty Cycle **Note:** 50% input duty cycle.	D_C	20/80% T_R/T_F<10% of period (Single-Ended input clock)	45	50	55	%
Minimum Input Clock Slew Rate	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	20–80%	—	—	350	ps
Minimum Input Pulse Width	T_W		360	—	—	ps
Propagation Delay	T_{PLH}, T_{PHL}		600	800	1000	ps
Output to Output Skew[1]	T_{SK}		—	25	60	ps
Part to Part Skew[2]	T_{PS}	Differential	—	—	150	ps
Power Supply Noise Rejection[3]	PSRR	10 kHz sinusoidal noise	—	–65	—	dBc
		100 kHz sinusoidal noise	—	–62.5	—	dBc
		500 kHz sinusoidal noise	—	–60	—	dBc
		1 MHz sinusoidal noise	—	–55	—	dBc

Notes:

1. Output-to-output skew specified for outputs with identical configuration.
2. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
3. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DD} (3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

Table 6. Additive Jitter, Differential Clock Input

V_{DD}	Input[1,2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (Single-Ended, Peak-to-Peak)	Differential 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	725	Differential	0.15	0.637	LVPECL	45	65
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
2.5	725	Differential	0.15	0.637	LVPECL	45	65
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185

Notes:
1. For best additive jitter results, use the fastest slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

Table 7. Additive Jitter, Single-Ended Clock Input

V_{DD}	Input[1,2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (single-ended, peak to peak)	SE 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185

Notes:
1. For best additive jitter results, use the fastest slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

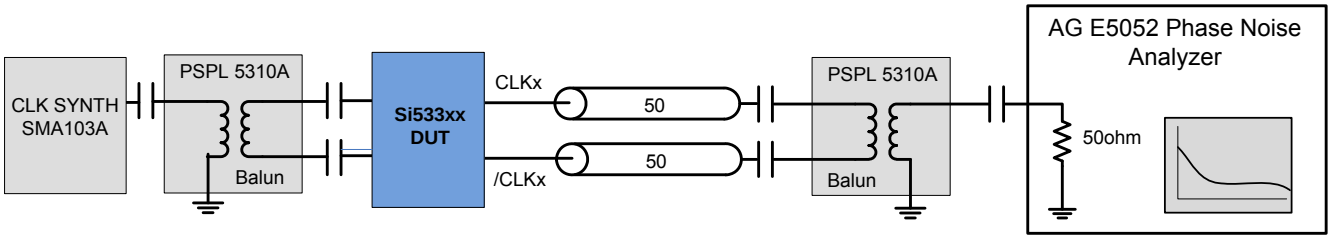


Figure 1. Differential Measurement Method Using a Balun

Table 8. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
32-eLQFP Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	54.9	°C/W
32-eLQFP Thermal Resistance, Junction to Case	θ_{JC}	Still air	10.0	°C/W
32-QFN Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	99.6	°C/W
32-QFN Thermal Resistance, Junction to Case	θ_{JC}	Still air	10.3	°C/W

Table 9. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	V_{DD}		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	V_{DD}+ 0.3	V
Output Voltage	V_{OUT}		—	—	V_{DD}+ 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	—	—	2000	V
ESD Sensitivity	CDM		—	—	500	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53325 is an ultra low jitter dual 1:5 LVPECL buffer. The device has a universal input that accepts most common differential or LVCMOS input signals.

2.1. Universal, Any-Format Input

The universal input stage enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 10 and 11 summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended as low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

Table 10. LVPECL, LVCMOS, and LVDS Input Clock Options

	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	No	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

Table 11. HCSL and CML Input Clock Options

	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	Yes (3.3 V)	Yes (3.3 V)	Yes	No

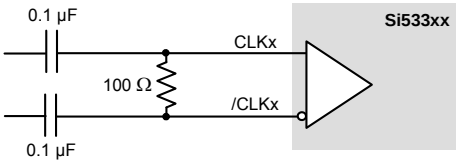


Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination

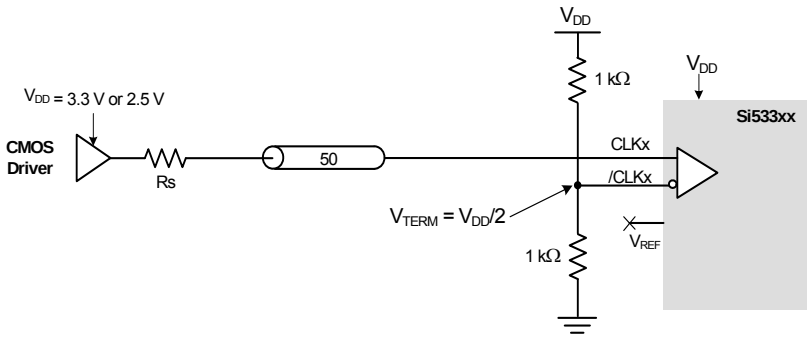
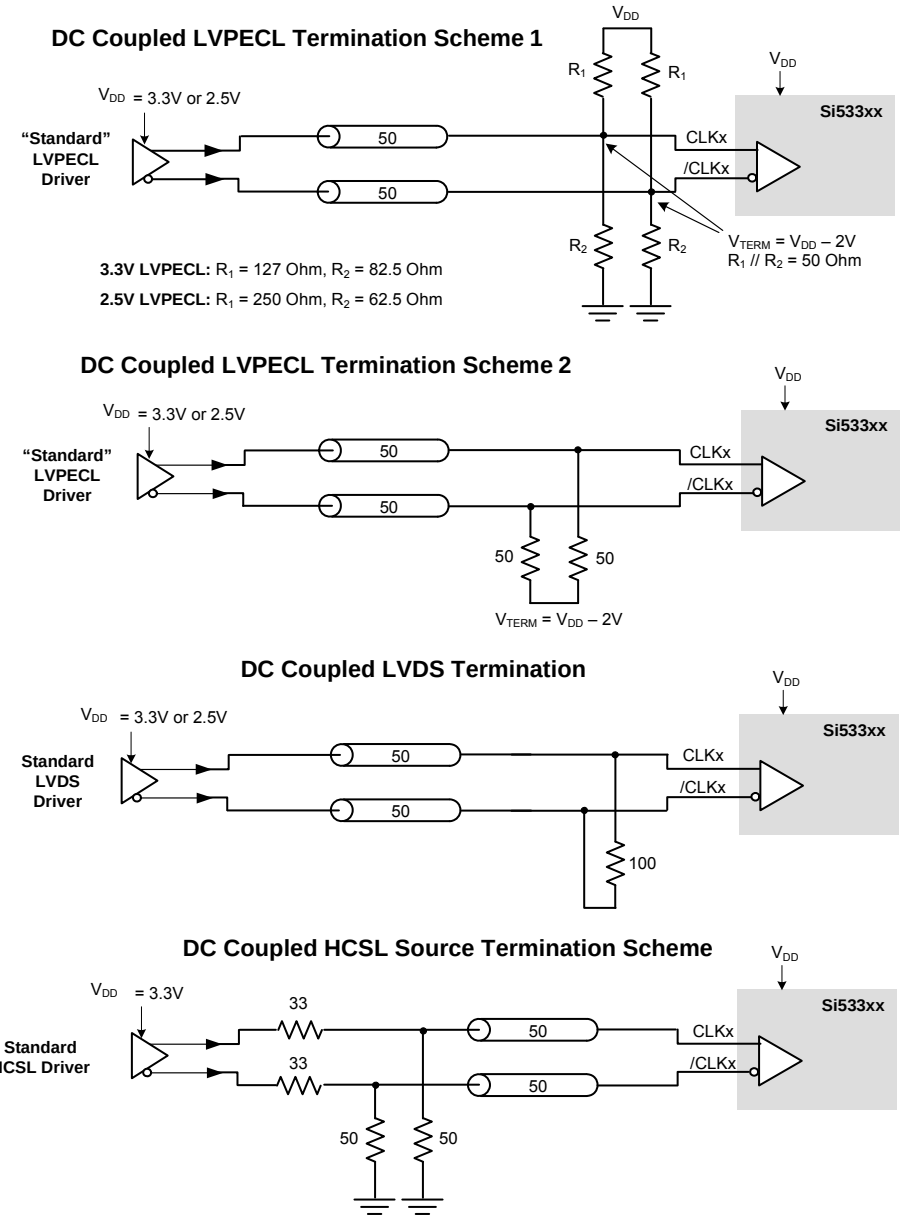


Figure 3. LVCMOS DC-Coupled Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 4. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The non-inverting input is biased with a 18.75 kΩ pull-down to GND and a 75 kΩ pull-up to V_{DD}. The inverting input is biased with a 75 kΩ pull-up to V_{DD}.

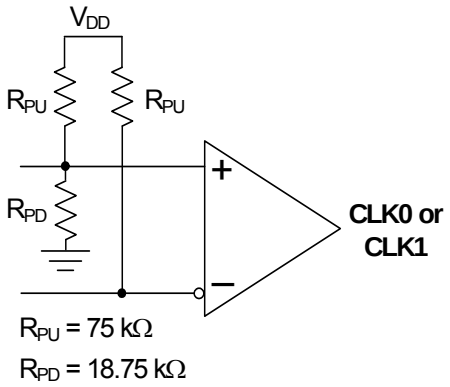


Figure 5. Input Bias Resistors

2.3. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused outputs should be left unconnected.

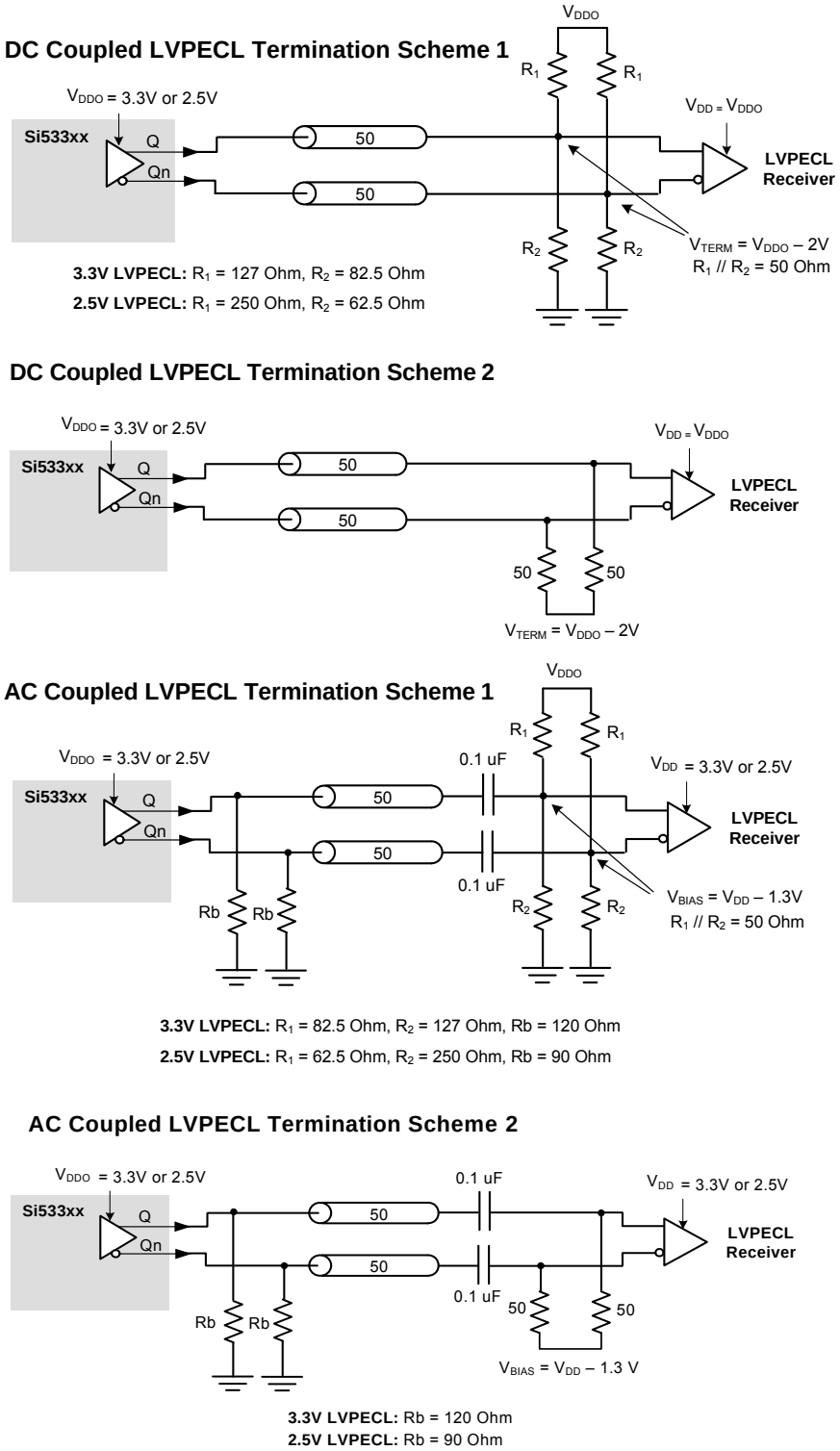


Figure 6. LVPECL Output Termination

2.4. AC Timing Waveforms

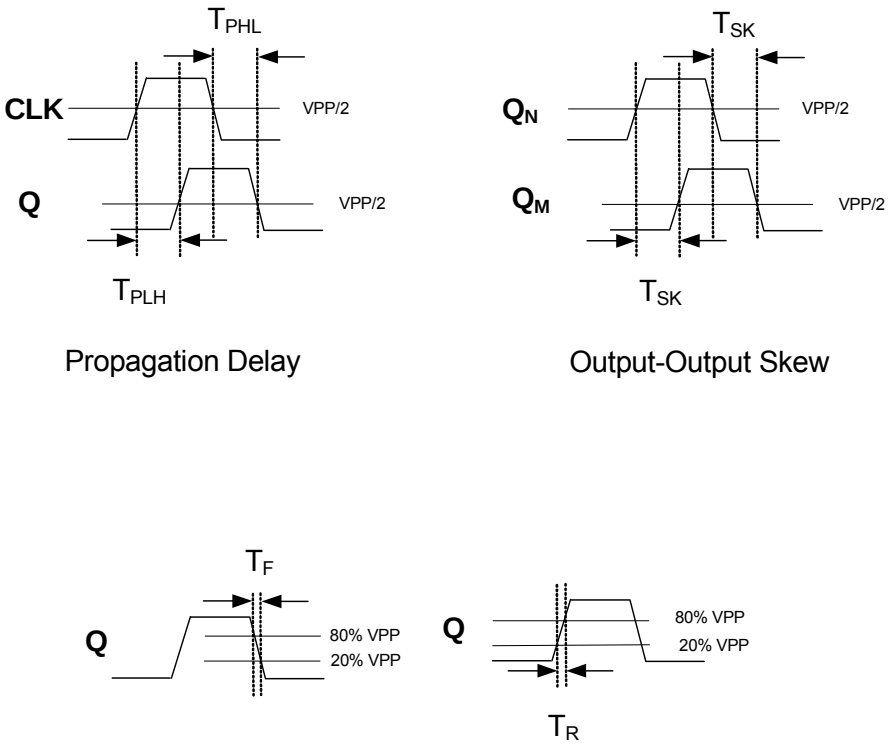


Figure 7. AC Waveforms

2.5. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

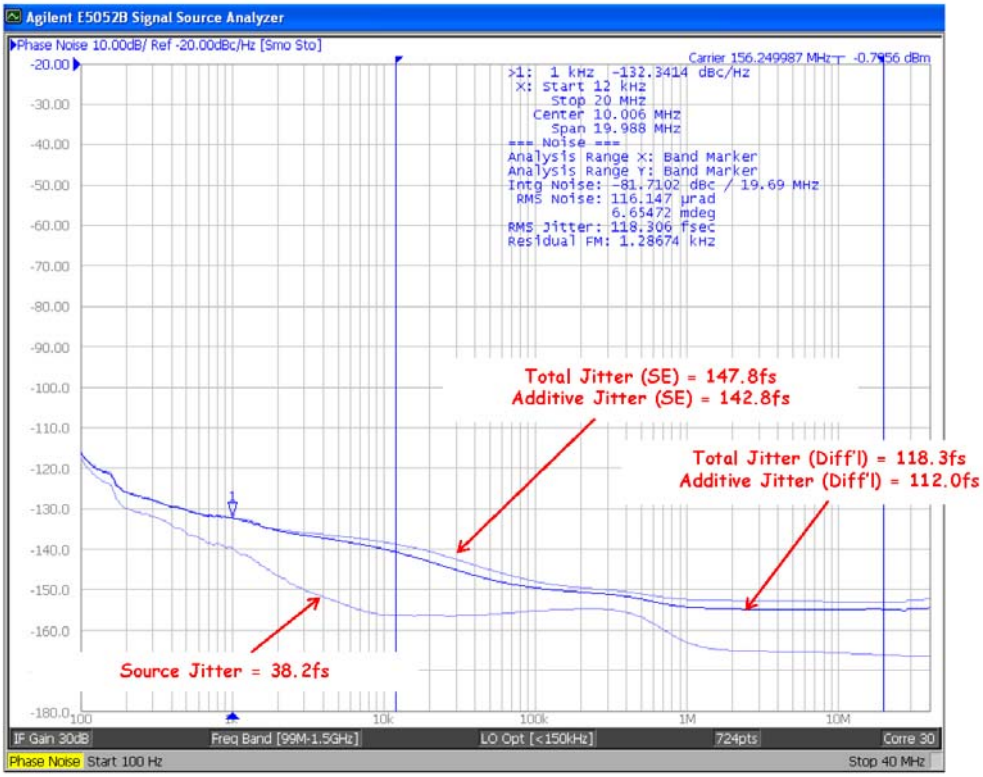
Source Jitter: Reference clock phase noise.

Total Jitter (SE): Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

Total Jitter (Diff): Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 5.

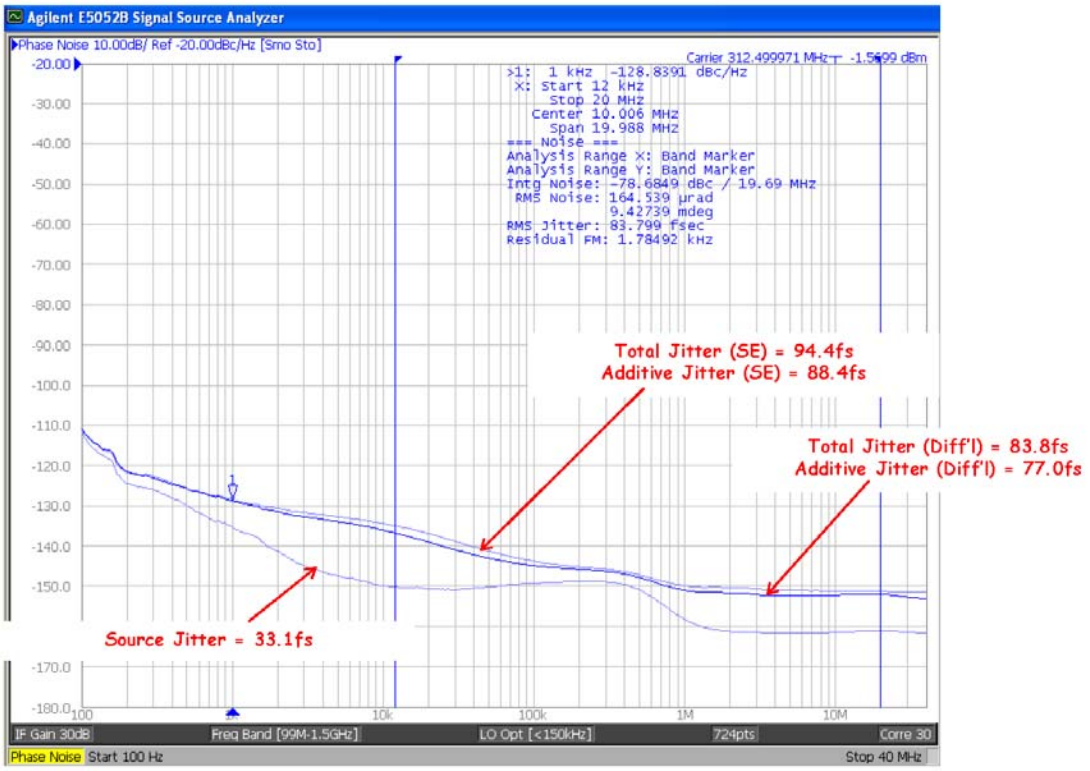
Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



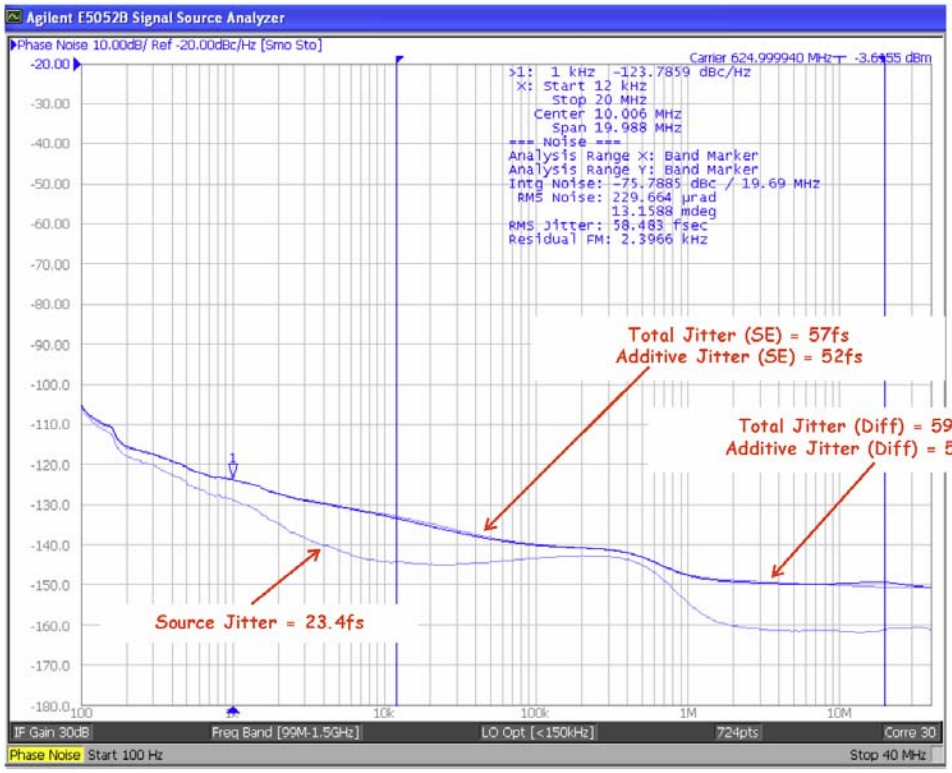
Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

Figure 8. Source Jitter (156.25 MHz)



Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
312.5	1.0	33.10	94.39	88.39	83.80	76.99

Figure 9. Single-Ended Total Jitter (312.5 MHz)



Frequency (MHz)	Diff Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff) (fs)	Additive Jitter (Diff) (fs)
625	1.0	23	57	52	59	54

Figure 10. Differential Total Jitter (625 MHz)

2.6. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

3. Pin Description: 32-eLQFP, 32-QFN

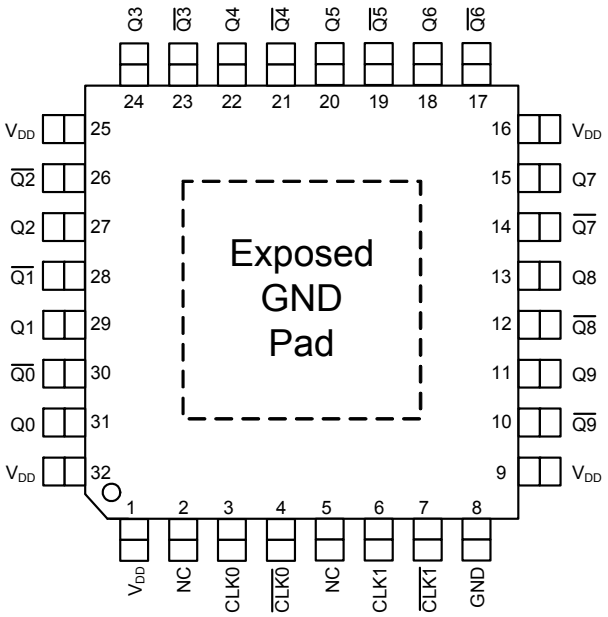


Figure 11. 32-eLQFP Pin Diagram (Top View)

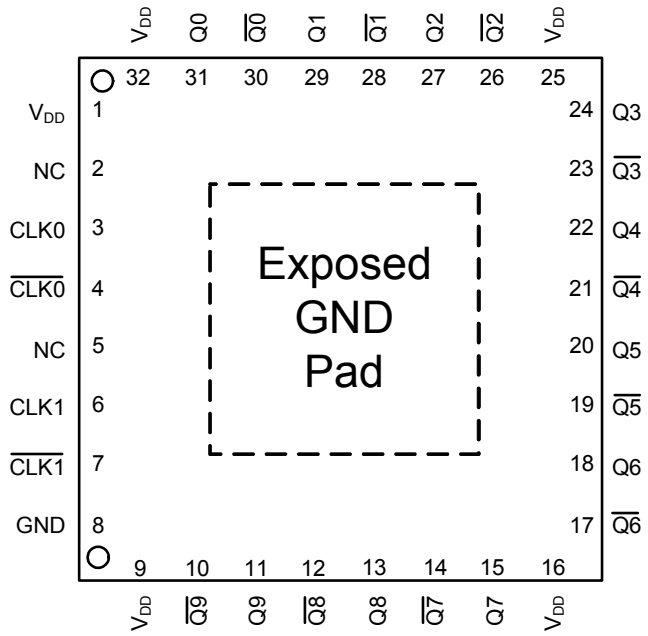


Figure 12. 32-QFN Pin Diagram (Top View)

Table 12. Si53325 32-eLQFP and 32-QFN Pin Descriptions

Pin #	Name	Type*	Description
1	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
2	NC	—	No connect. Leave this pin unconnected.
3	CLK0	I	Input clock 0.
4	$\overline{CLK0}$	I	Input clock 0 (complement).
5	NC	—	No connect. Leave this pin unconnected.
6	CLK1	I	Input clock 1.
7	$\overline{CLK1}$	I	Input clock 1 (complement).
8	GND	GND	Ground.
9	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
10	$\overline{Q9}$	O	Output clock 9 (complement).
11	Q9	O	Output clock 9.
12	$\overline{Q8}$	O	Output clock 8 (complement).
13	Q8	O	Output clock 8.
14	$\overline{Q7}$	O	Output clock 7 (complement).
15	Q7	O	Output clock 7.
16	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
17	$\overline{Q6}$	O	Output clock 6 (complement).
18	Q6	O	Output clock 6.
19	$\overline{Q5}$	O	Output clock 5 (complement).
20	Q5	O	Output clock 5.
21	$\overline{Q4}$	O	Output clock 4 (complement).
22	Q4	O	Output clock 4.
23	$\overline{Q3}$	O	Output clock 3 (complement).
24	Q3	O	Output clock 3.
25	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
26	$\overline{Q2}$	O	Output clock 2 (complement).

Table 12. Si53325 32-eLQFP and 32-QFN Pin Descriptions (Continued)

Pin #	Name	Type*	Description
27	Q2	O	Output clock 2.
28	$\overline{Q1}$	O	Output clock 1 (complement).
29	Q1	O	Output clock 1.
30	$\overline{Q0}$	O	Output clock 0 (complement).
31	Q0	O	Output clock 0.
32	V_{DD}	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
33	Exposed ground pad	GND	Ground Pad. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.
*Pin types are: I = input, O = output, P = power, GND = ground.			

4. Ordering Guide

Part Number	Package	PB-Free, ROHS-6	Temperature
Si53325-B-GQ	32-eLQFP	Yes	–40 to 85 °C
Si53325-B-GM	32-QFN	Yes	–40 to 85 °C

5. Package Outline

5.1. 32-eLQFP Package Diagram

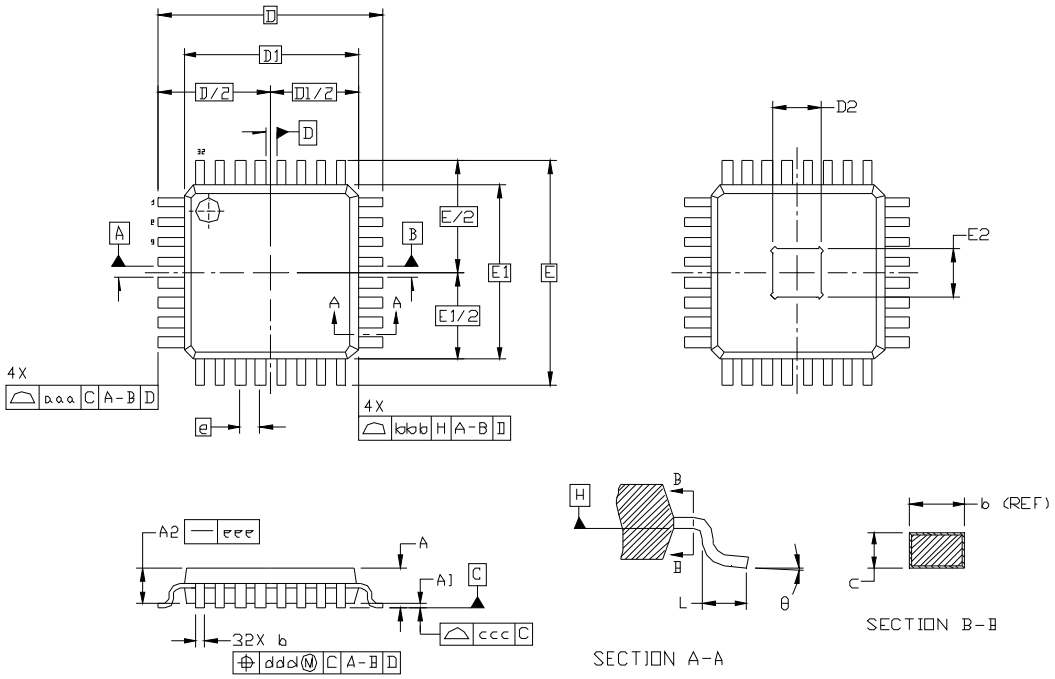


Figure 13. Si53325 32-eLQFP Package Diagram

Table 13. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
D2	1.87	1.92	1.97
e	0.80 BSC		
E	9.00 BSC		

Dimension	Min	Nom	Max
E1	7.00 BSC		
E2	1.87	1.92	1.97
L	0.45	0.60	0.75
Θ	0°	3.5°	7°
aaa	0.20		
bb	0.20		
ccc	0.10		
dddd	0.20		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.2. 32-QFN Package Diagram

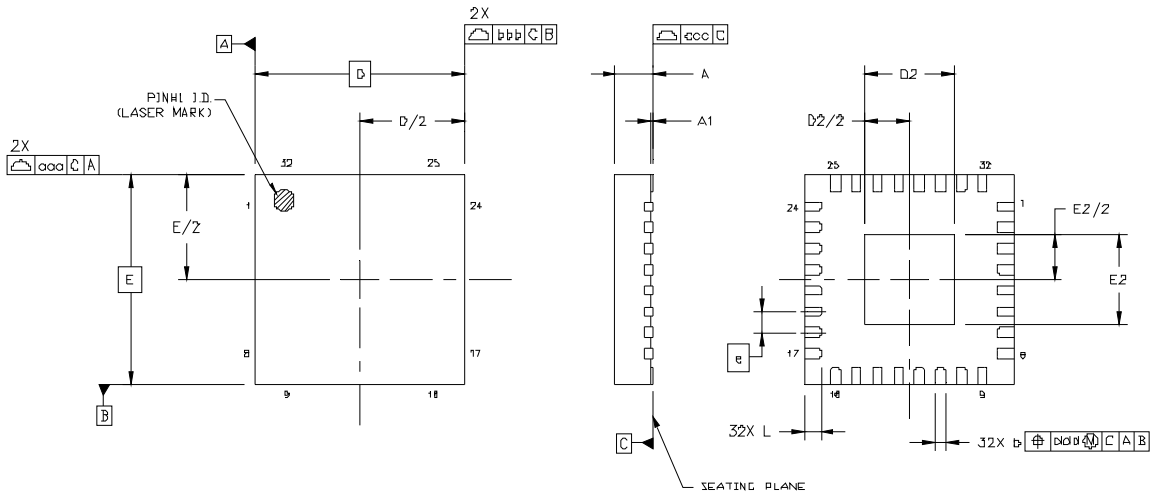


Figure 14. Si53325 32-QFN Package Diagram

Table 14. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.20	0.25	0.30
D	5.00 BSC		
D2	2.00	2.15	2.30
e	0.50 BSC		
E	5.00 BSC		
E2	2.00	2.15	2.30
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC Solid State Outline MO-220.

6. PCB Land Pattern

6.1. 32-eLQFP Package Land Pattern

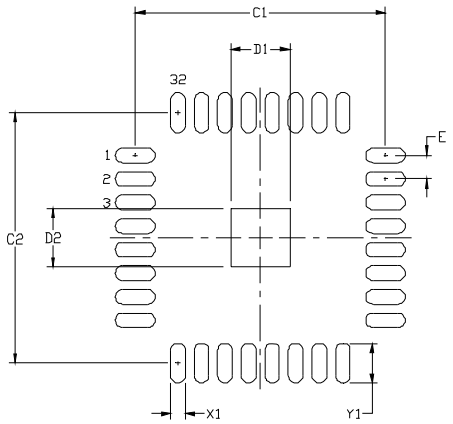


Figure 15. Si53325 32-eLQFP Package Land Pattern

Table 15. PCB Land Pattern

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
D1	1.84	2.00
D2	1.84	2.00
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A single 1.5 x 1.5 mm stencil aperture should be used for the center ground pad to achieve between 50-60% solder coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2. 32-QFN Package Land Pattern

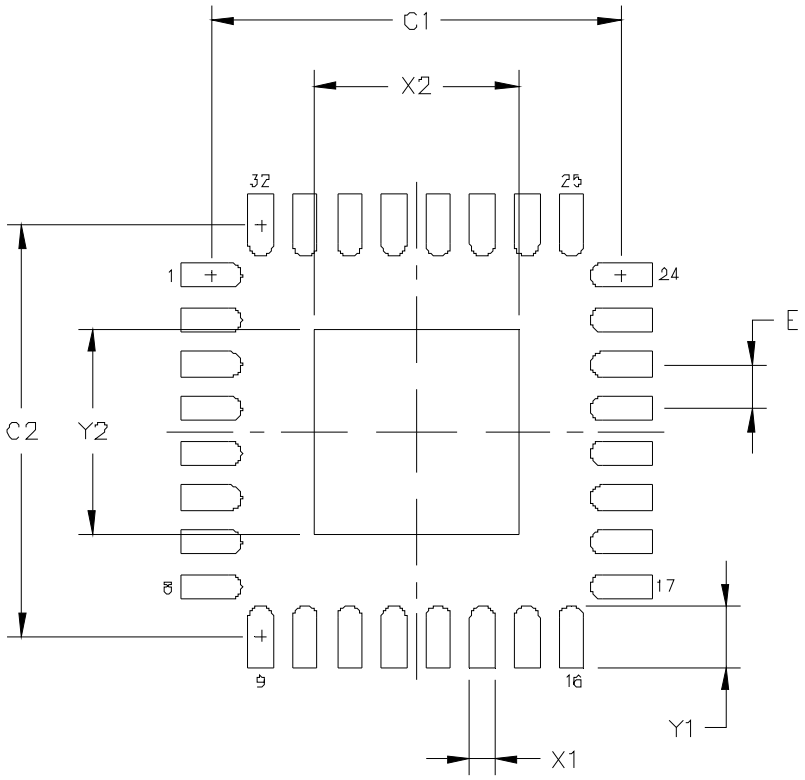


Figure 16. Si53325 32-QFN Package Land Pattern

Table 16. PCB Land Pattern

Dimension	Min	Max
C1	4.52	4.62
C2	4.52	4.62
E	0.50 BSC	
X1	0.20	0.30

Dimension	Min	Max
X2	2.20	2.30
Y1	0.59	0.69
Y2	2.20	2.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

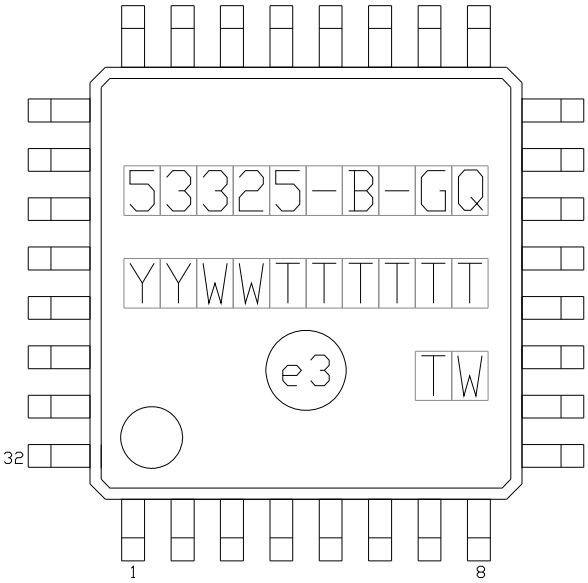
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Markings

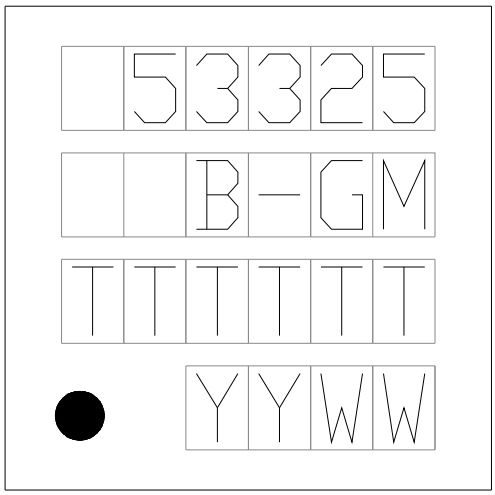
7.1. Si53325 32-eLQFP Top Marking



7.2. Top Marking Explanation (32-eLQFP)

Mark Method:	Laser	
Font Size:	1.9 Point (26 mils) Right-Justified	
Line 1 Marking:	Device Part Number	**53325-B-GQ**
Line 2 Marking:	YY = Year WW = Work Week	Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.3 mm Diameter Center-Justified	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	**TW**

7.3. Si53325 32-QFN Top Marking



7.4. Top Marking Explanation (32-QFN)

Mark Method:	Laser	
Font Size:	2.0 Point (28 mils) Center-Justified	
Line 1 Marking:	Device Part Number	**53325**
Line 2 Marking:	Device Revision/Type	**B-GM**
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 4 Marking	Circle = 0.50 mm Diameter Lower-Left Justified	Pin 1 Identifier
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

Document Change List

Revision 0.4 to 1.0

- Update operating conditions, including LVCMOS and HCSL voltage support.
- Removed voltage reference feature.
- Updated Table 2, “Input Clock Specifications,” on page 3.
- Updated Table 3, “DC Common Characteristics,” on page 3.
- Updated Table 4, “Output Characteristics (LVPECL),” on page 4.
- Updated Table 10, “LVPECL, LVCMOS, and LVDS Input Clock Options,” on page 7.
- Updated output voltage specifications.
- Improved data for additive jitter specifications.
- Improved typical phase noise plots.
- Updated input/output termination recommendations.
- Improved performance specifications with more detail.
- Added pin type description to the pin descriptions table.
- Updated ESD specifications.

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