

Low Jitter and Skew 10 to 220 MHz Zero Delay Buffer (ZDB)

Key Features

- 10 to 220 MHz operating frequency range
- Low output clock skew: 45ps-typ
- Low output clock jitter:
 - 25 ps-typ cycle-to-cycle jitter
 - 15 ps-typ period jitter
- Low part-to-part output skew: 90 ps-typ
- Wide 2.5 V to 3.3 V power supply range
- Low power dissipation:
 - 20 mA-max at 66 MHz and VDD=3.3 V
 - 18 mA-max at 66 MHz and VDD=2.5V
- One input drives 8 outputs
- Multiple configurations and drive options
- Select mode to bypass PLL or tri-state outputs
- SpreadThru™ PLL that allows use of SSCG
- Available in 16-pin SOIC and TSSOP packages
- Available in Commercial and Industrial grades

Applications

- Printers, MFPs and Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Datacom and Telecom
- High-SpeedDigital Embedded Systems

Description

The SL23EP08 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to nine (9) clock outputs from one (1) reference input clock, for high speed clock distribution applications.

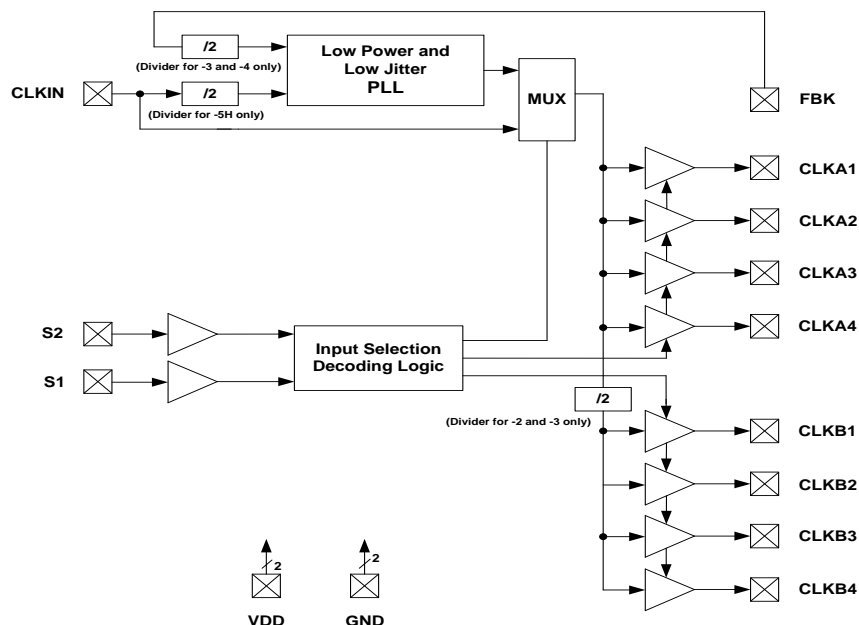
The product has an on-chip PLL and a feedback pin (FBK) which can be used to obtain feedback from any one of the output clocks. The SL23EP08 has two (2) clock driver banks each with four (4) clock outputs. These outputs are controlled by two (2) select input pins S1 and S2. When only four (4) outputs are needed, four (4) bank-B output clock buffers can be tri-stated to reduce power dissipation and jitter. The select inputs can also be used to tri-state both banks A and B or drive them directly from the input bypassing the PLL and making the product behave like a Non-Zero Delay Buffer (NZDB). The product also offers various 1X, 2X and 4X frequency options at the output clocks. Refer to the “Product Configuration Table” for the details.

The high-drive version operates up to 220MHz and 200MHz at 3.3V and 2.5V power supplies respectively.

Benefits

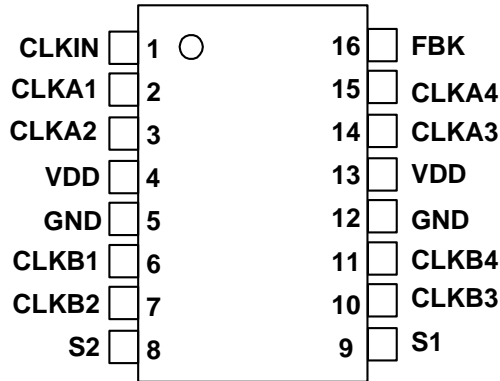
- Up to eight (8) distribution of input clock
- Standard and High-Dirive levels to control impedance level, frequency range and EMI
- Low power dissipation, jitter and skew
- Low cost

Block Diagram



16-Pin SOIC and TSSOP

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | CLKIN | Input | Reference Frequency Clock Input. 5V tolerant input. Weak pull-down (250kΩ). |
| 2 | CLKA1 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 3 | CLKA2 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 4 | VDD | Power | 3.3V or 2.5V Power Supply. |
| 5 | GND | Power | Power Ground. |
| 6 | CLKB1 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 7 | CLKB2 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 8 | S2 | Input | Select Input, select pin S2. Weak pull-up (250kΩ). |
| 9 | S1 | Input | Select Input, select pin S1. Weak pull-up (250kΩ). |
| 10 | CLKB3 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 11 | CLKB4 | Output | Buffered Clock Output, Bank B. Weak pull-down (250kΩ). |
| 12 | GND | Power | Power Ground. |
| 13 | VDD | Power | 3.3V or 2.5V Power Supply. |
| 14 | CLKA3 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 15 | CLKA4 | Output | Buffered Clock Output, Bank A. Weak pull-down (250kΩ). |
| 16 | FBK | Output | PLL Feedback input. |

General Description-

The SL23EP08 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces nine (9) output clock drivers tracking the input reference clock for systems requiring clock distribution.

In addition to CLKOUT that is used for internal PLL feedback, there are two (2) banks with four (4) outputs in each bank, bringing the number of total available output clocks to nine (9).

Input and output Frequency Range-

The input and output frequency range is the same. But, the frequency range depends on VDD and drive levels as given in the below Table 1.

| VDD(V) | Drive | Min(MHz) | Max(MHz) |
|--------|-------|----------|----------|
| 3.3 | HIGH | 10 | 220 |
| 3.3 | STD | 10 | 167 |
| 2.5 | HIGH | 10 | 200 |
| 2.5 | STD | 10 | 133 |

Table 1. Input/Output Frequency Range

If the input clock frequency is less than 2 MHz or floating, this is detected by an input frequency detection circuitry and all eight (8) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 25 μ A supply current.

SpreadThru™ Feature-

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL23EP08 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency

Select Input Control-

The SL23EP08 provides two (2) input select control pins called S1 and S2. This feature enables users to select various states of output clock banks-A and bank-B, output source and PLL shutdown features as shown in the Table 2.

The S1 (Pin-9) and S2 (Pin-8) inputs include 250 k Ω weak pull-down resistors to GND.

PLL Bypass Mode

If the S1 and S2 pins are logic Low(0) and High(1) respectively, the on-chip PLL is shutdown and bypassed, and all the nine output clocks bank A, bank B and CLKOUT clocks are driven by directly from the reference input clock. In this operation mode SL23EP08 works like a non-ZDB product.

High and Low-Drive Product Options -

The SL23EP08 is offered with High-Drive “-1H” and Standard-Drive “-1” options. These drive options enable the users to control load levels, frequency range and EMI control. Refer to the AC electrical tables for the details.

Skew and Zero Delay -

All outputs should drive the similar load to achieve output-to-output skew and input-to-output specifications given in the AC electrical tables. However, Zero delay between input and outputs can be adjusted by changing the loading of CLKOUT relative to the banks A and B clocks since CLKOUT is the feedback to the PLL.

Power Supply Range (VDD)-

The SL23EP08 is designed to operate in a wide power supply range from 2.3V (Min) to 3.3V (Max). An internal on-chip voltage regulator is used to supply PLL constant power supply of 1.8V, leading to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation. Contact SLI for 1.8V power supply version ZDB called SL23EPL08.

| S2 | S1 | Clock A1-A4 | Clock B1-B4 | CLKOUT | Output Source | PLL Shutdown and Bypass |
|----|----|-----------------------|-----------------------|------------|---------------|-------------------------|
| 0 | 0 | Tri-state | Tri-state | Driven | PLL | Yes |
| 0 | 1 | Driven | Tri-state | Driven | PLL | No |
| 1 | 0 | Driven ^[1] | Driven ^[1] | Driven (4) | Reference | Yes |
| 1 | 1 | Driven | Driven | Driven | PLL | No |

Table 2. Select Input Decoding

| Device | Feedback From | Bank-A Frequency | Bank-B Frequency |
|-------------|------------------|------------------|--------------------------|
| SL23EP08-1 | Bank-A or Bank-B | Reference | Reference |
| SL23EP08-1H | Bank-A or Bank-B | Reference | Reference |
| SL23EP08-2 | Bank-A | Reference | Reference/2 |
| SL23EP08-2 | Bank-B | 2x Reference | Reference |
| SL23EP08-3 | Bank-A | 2X Reference | Reference ^[2] |
| SL23EP08-3 | Bank-B | 4X Reference | 2X Reference |
| SL23EP08-4 | Bank-A or Bank-B | 2X Reference | 2X Reference |
| SL23EP08-5H | Bank-A or Bank-B | Reference /2 | Reference /2 |

Table 3. Available SL23EP08 Configurations

Notes:

1. Outputs are inverted on SL23EP08-2 and SL23EP08-3 in PLL bypass mode when S2=1 and S1=0.
2. Output phase is either 0° or 180° with respect to CLKIN input. If phase integrity is required, use the SL23EP08-2.

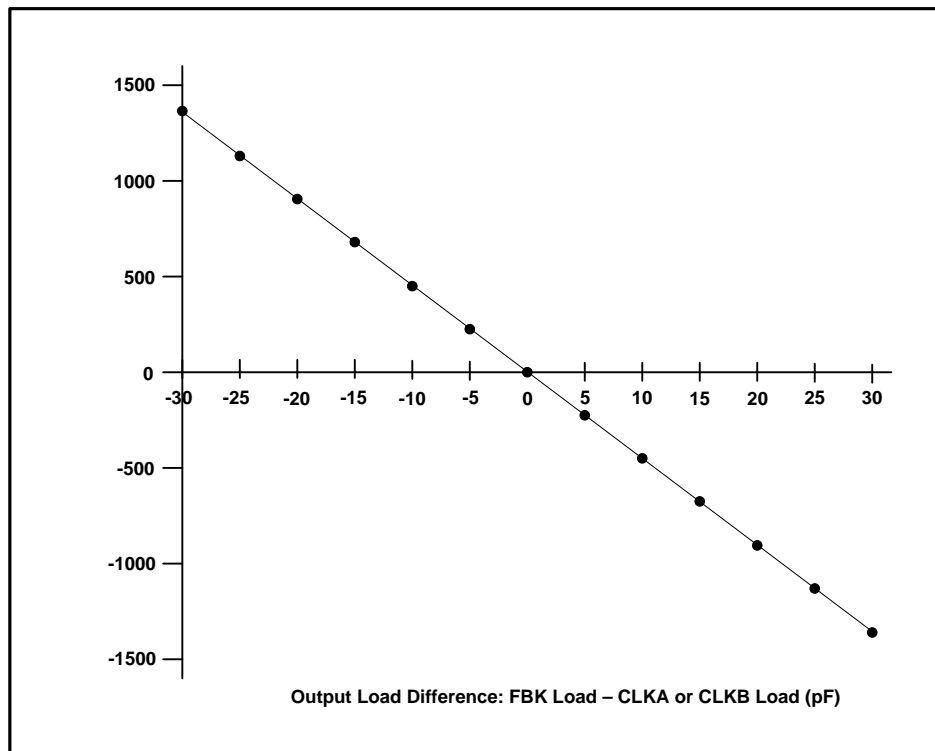


Figure 1. CLKIN Input to CLKA and CLKB Delay

Absolute Maximum Ratings

| Description | Condition | Min. | Max. | Unit |
|---------------------|-----------|------|------|------|
| Supply voltage, VDD | | -0.5 | 4.6 | V |

| | | | | |
|-------------------------------|--------------------------------|-------|---------|----|
| All Inputs and Outputs | | - 0.5 | VDD+0.5 | V |
| Ambient Operating Temperature | In operation, C-Grade | 0 | 70 | °C |
| Ambient Operating Temperature | In operation, I-Grade | - 40 | 85 | °C |
| Storage Temperature | No power is applied | - 65 | 150 | °C |
| Junction Temperature | In operation, power is applied | - | 125 | °C |
| Soldering Temperature | | - | 260 | °C |
| ESD Rating (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |

Operating Conditions: Unless otherwise stated VDD=2.5V to 3.3V and for both C and I Grades

| Symbol | Description | Condition | Min. | Max. | Unit |
|--------|--------------------------------|--|------|------|------|
| VDD3.3 | 3.3V Supply Voltage | 3.3V+/-10% | 3.0 | 3.6 | V |
| VDD2.5 | 2.5V Supply Voltage | 2.5V+/-10% | 2.3 | 2.7 | V |
| TA | Operating Temperature(Ambient) | Commercial | 0 | 70 | °C |
| | | Industrial | -40 | 85 | °C |
| CLOAD | Load Capacitance | <100 MHz, 3.3V with Standard or High drive | - | 30 | pF |
| | | <100 MHz, 2.5V with High drive | - | 30 | pF |
| | | <133.3 MHz, 3.3V with Standard or High drive | - | 22 | pF |
| | | <133.3 MHz, 2.5V with High drive | - | 22 | pF |
| | | <133.3 MHz, 2.5V with Standard drive | - | 15 | pF |
| | | >133.3 MHz, 3.3V with Standard or High drive | - | 15 | pF |
| | | >133.3 MHz, 2.5V with High drive | - | 15 | pF |
| CIN | Input Capacitance | S1, S2 and CLKIN pins | - | 5 | pF |
| CLBW | Closed-loop bandwidth | 3.3V, (typical) | 1.2 | | MHz |
| | | 2.5V, (typical) | 0.8 | | MHz |
| ZOUT | Output Impedance | 3.3V, (typical), High drive | 29 | | Ω |
| | | 3.3V, (typical), Standard drive | 41 | | Ω |
| | | 2.5V, (typical), High drive | 37 | | Ω |
| | | 2.5V, (typical), Standard drive | 41 | | Ω |

DC Electrical Specifications (VDD=3.3V): Unless otherwise stated for both C and I Grades

| Symbol | Description | Condition | Min. | Max. | Unit |
|--------|-------------|-----------|------|------|------|
|--------|-------------|-----------|------|------|------|

| | | | | | |
|-------|---|-----------------------------------|-------|----------------------|----|
| VDD | Supply Voltage | | 2.970 | 3.630 | V |
| VIL | Input LOW Voltage | | – | 0.8 | V |
| VIH | Input HIGH Voltage | | 2.0 | V _{DD} +0.3 | V |
| IIL | Input Leakage Current | 0 < V _{IN} < 0.8V | – | ±10 | µA |
| IIH | Input HIGH Current | V _{IN} = V _{DD} | – | 100 | µA |
| VOL | Output LOW Voltage | IOL = 8 mA (standard drive) | – | 0.4 | V |
| | | IOL = 12 mA (high drive) | – | 0.4 | V |
| VOH | Output HIGH Voltage | IOH = –8 mA (standard drive) | 2.4 | – | V |
| | | IOH = –12 mA (high drive) | 2.4 | – | V |
| IDDPD | Power Down Supply Current CLKIN<2MHz | CLKIN = 0 MHz (C-Grade) | – | 12 | µA |
| | | CLKIN = 0 MHz (I-Grade) | – | 25 | µA |
| IDD | Power Supply Current | All Outputs CL=0, 66-MHz CLKIN | – | 20 | mA |

DC Electrical Specifications (VDD=2.5V): Unless otherwise stated for both C and I Grades

| Symbol | Description | Condition | Min. | Max. | Unit. |
|--------|---|-----------------------------------|-----------------------|-----------------------|-------|
| VDD | Supply Voltage | | 2.3 | 2.7 | V |
| VIL | Input LOW Voltage | | – | 0.7 | V |
| VIH | Input HIGH Voltage | | 1.7 | V _{DD} + 0.3 | V |
| IIL | Input Leakage Current | 0<V _{IN} < 0.8V | – | 10 | µA |
| IIH | Input HIGH Current | V _{IN} = V _{DD} | – | 100 | µA |
| VOL | Output LOW Voltage | IOL = 8 mA (standard drive) | – | 0.5 | V |
| | | IOL = 12 mA (high drive) | – | 0.5 | V |
| VOH | Output HIGH Voltage | IOH = –8 mA (standard drive) | V _{DD} – 0.6 | – | V |
| | | IOH = –12 mA (high drive) | V _{DD} – 0.6 | – | V |
| IDDPD | Power Down Supply Current CLKIN<2MHz | CLKIN = 0 MHz (C-Grade) | – | 12 | µA |
| | | CLKIN = 0 MHz (I-Grade) | – | 25 | µA |
| IDD | Power Supply Current | All Outputs CL=0, 66-MHz CLKIN | – | 18 | mA |

AC Electrical Specifications: VDD=3.3V+/-10% and 0°C to +70°C Operation (Commercial Grade)

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|--------|---|---|------|------|------|------|
| FOUT-1 | Output Frequency | CL=30pf, All devices | 10 | - | 160 | MHz |
| FOUT-2 | Output Frequency | CL=20pF, -1H and -5H versions | 10 | - | 220 | MHz |
| FOUT-2 | Output Frequency | CL=15pF, -1,-2,-3 and -4 versions | 10 | - | 200 | MHz |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=66.6MHz and Measured at VDD/2 | 40.0 | 50.0 | 60.0 | % |
| DC-2 | Duty Cycle, -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT<66.6MHz and Measured at VDD/2 | 45.0 | 50.0 | 55.0 | % |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| DC-2 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| tr/f-1 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.6 | ns |
| tr/f-2 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1,1H and -5H versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1H and -5H versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.0 | ns |
| SKW-1 | Output-to-Output on same bank A or B. All versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-2 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-3 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 130 | 300 | ps |
| SKW-4 | Device-to-Device Skew. All versions | All outputs are equally loaded. Measured at VDD/2 and FBK pin | - | 180 | 500 | ps |
| tCFD | CLKIN to FBK Rising Edge Delay | All outputs are equally loaded. Measured at VDD/2 | -200 | - | 200 | ps |
| t2 | Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge ^[2] (Measured at VDD/2) | PLL Bypass mode | 1.5 | - | 4.4 | ns |
| | | PLL enabled @ 3.3V | -100 | - | 100 | ps |
| | | PLL enabled @2.5V | -200 | - | 200 | ps |
| t3 | Part-to-Part Skew ^[2] (Measured at VDD/2) | Measured at VDD/2. Any output to any output, 3.3V supply | - | - | ±150 | ps |
| | | Measured at VDD/2. Any output to any output, 2.5V supply | - | - | ±300 | ps |
| tLOCK | PLL Lock Time | Valid on all clock pins from VDD=2.97V | - | - | 1.0 | ms |

AC Electrical Specifications: VDD=3.3V+/-10% and -40°C to +85°C Operation (Industrial Grade)

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|--------|---|---|------|------|------|------|
| FOUT-1 | Output Frequency | CL=30pf, All devices | 10 | - | 160 | MHz |
| FOUT-2 | Output Frequency | CL=20pF, -1H and -5H versions | 10 | - | 220 | MHz |
| FOUT-2 | Output Frequency | CL=15pF, -1,-2,-3 and -4 versions | 10 | - | 200 | MHz |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=66.6MHz and Measured at VD/2 | 40.0 | 50.0 | 60.0 | % |
| DC-2 | Duty Cycle, -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT<66.6MHz and Measured at VDD/2 | 45.0 | 50.0 | 55.0 | % |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| DC-2 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| tr/f-1 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.6 | ns |
| tr/f-2 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1,1H and -5H versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1H and -5H versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.0 | ns |
| SKW-1 | Output-to-Output on same bank A or B. All versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-2 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-3 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 130 | 300 | ps |
| SKW-4 | Device-to-Device Skew. All versions | All outputs are equally loaded. Measured at VDD/2 and FBK pin | - | 180 | 500 | ps |
| tCFD | CLKIN to FBK Rising Edge Delay | All outputs are equally loaded. Measured at VDD/2 | -200 | - | 200 | ps |
| t2 | Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge ^[2] (Measured at VDD/2) | PLL Bypass mode | 1.5 | - | 4.4 | ns |
| | | PLL enabled @ 3.3V | -100 | - | 100 | ps |
| | | PLL enabled @2.5V | -200 | - | 200 | ps |
| t3 | Part-to-Part Skew ^[2] (Measured at VDD/2) | Measured at VDD/2. Any output to any output, 3.3V supply | - | - | ±150 | ps |
| | | Measured at VDD/2. Any output to any output, 2.5V supply | - | - | ±300 | ps |
| tLOCK | PLL Lock Time | Valid on all clock pins from VDD=2.97V | - | - | 1.0 | ms |

AC Electrical Specifications: VDD=2.5V+/-10% and 0°C to +70°C Operation (Commercial Grade)

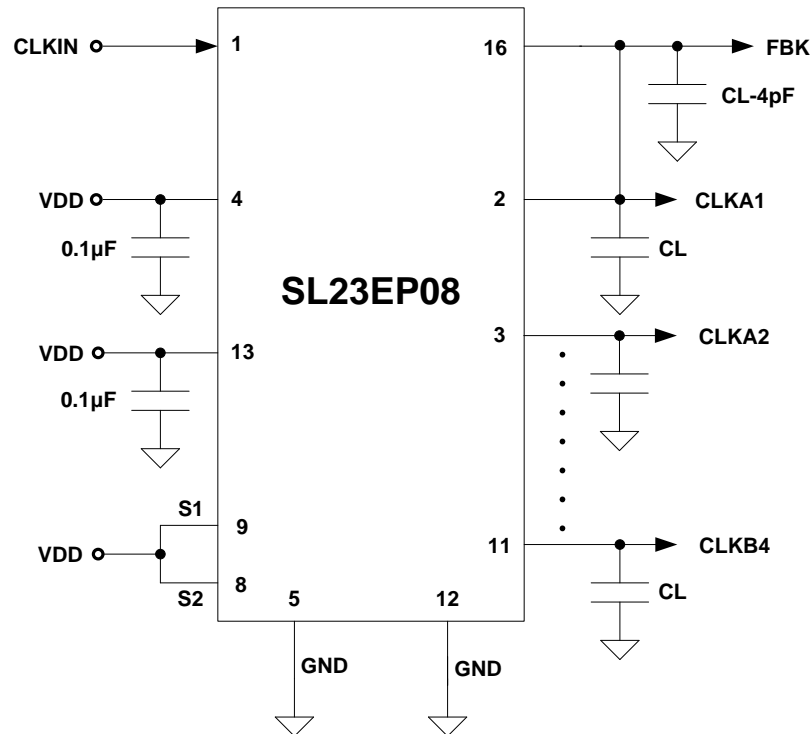
| Symbol | Description | Condition | Min | Typ | Max | Unit |
|--------|---|---|------|------|------|------|
| FOUT-1 | Output Frequency | CL=30pf, All devices | 10 | - | 160 | MHz |
| FOUT-2 | Output Frequency | CL=20pF, -1H and -5H versions | 10 | - | 220 | MHz |
| FOUT-2 | Output Frequency | CL=15pF, -1,-2,-3 and -4 versions | 10 | - | 200 | MHz |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=66.6MHz and Measured at VDD/2 | 40.0 | 50.0 | 60.0 | % |
| DC-2 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT<66.6MHz and Measured at VDD/2 | 45.0 | 50.0 | 55.0 | % |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| DC-2 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| tr/f-1 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.6 | ns |
| tr/f-2 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1,1H and -5H versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1H and -5H versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.0 | ns |
| SKW-1 | Output-to-Output on same bank A or B. All versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-2 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-3 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 130 | 300 | ps |
| SKW-4 | Device-to-Device Skew. All versions | All outputs are equally loaded. Measured at VDD/2 and FBK pin | - | 180 | 500 | ps |
| tCFD | CLKIN to FBK Rising Edge Delay | All outputs are equally loaded. Measured at VDD/2 | -200 | - | 200 | ps |
| t2 | Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge ^[2] (Measured at VDD/2) | PLL Bypass mode | 1.5 | - | 4.4 | ns |
| | | PLL enabled @ 3.3V | -100 | - | 100 | ps |
| | | PLL enabled @2.5V | -200 | - | 200 | ps |
| t3 | Part-to-Part Skew ^[2] (Measured at VDD/2) | Measured at VDD/2. Any output to any output, 3.3V supply | - | - | ±150 | ps |
| | | Measured at VDD/2. Any output to any output, 2.5V supply | - | - | ±300 | ps |
| tLOCK | PLL Lock Time | Valid on all clock pins from VDD=2.97V | - | - | 1.0 | ms |

AC Electrical Specifications: VDD=2.5V+/-10% and -40°C to +85°C Operation (Industrial Grade)

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|--------|---|--|------|------|------|------|
| FOUT-1 | Output Frequency | CL=30pf, All devices | 10 | - | 160 | MHz |
| FOUT-2 | Output Frequency | CL=20pF, -1H and -5H versions | 10 | - | 220 | MHz |
| FOUT-2 | Output Frequency | CL=15pF, -1,-2,-3 and -4 versions | 10 | - | 200 | MHz |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=66.6MHz and Measured at VDD/2 | 40.0 | 50.0 | 60.0 | % |
| DC-2 | Duty Cycle, -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT<66.6MHz and Measured at VDD/2 | 45.0 | 50.0 | 55.0 | % |
| DC-1 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=30pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| DC-2 | Duty Cycle. -1, -2, -3,-4,-1H and -5H versions | CL=15pF, FOUT=120MHz and Measured at VDD/2 | TBD | TBD | TBD | % |
| tr/f-1 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.6 | ns |
| tr/f-2 | Rise and Fall Times. -1, -2, -3, and -4 versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1,1H and -5H versions | Measured between 0.8V and 2.0V CL=30pF | - | - | 1.2 | ns |
| tr/f-3 | Rise and Fall Times. -1H and -5H versions | Measured between 0.8V and 2.0V CL=15pF | - | - | 1.0 | ns |
| SKW-1 | Output-to-Output on same bank A or B. All versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-2 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 60 | 150 | ps |
| SKW-3 | Output Bank-A to Bank-B Skew. -1-4 and -5H versions | All outputs are equally loaded. Measured at VDD/2 | - | 130 | 300 | ps |
| SKW-4 | Device-to-Device Skew. All versions | All outputs are equally loaded. Measured at VDD/2 | - | 180 | 500 | ps |
| tCFD | CLKIN to FBK Rising Edge Delay | All outputs are equally loaded. Measured at VDD/2 | -200 | - | 200 | ps |
| t2 | Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge ^[2] (Measured at VDD/2) | PLL Bypass mode | 1.5 | - | 4.4 | ns |
| | | PLL enabled @ 3.3V | -100 | - | 100 | ps |
| | | PLL enabled @2.5V | -200 | - | 200 | ps |
| t3 | Part-to-Part Skew (Measured at VDD/2) | Measured at VDD/2. Any output to any output, 3.3V supply | - | - | ±150 | ps |
| | | Measured at VDD/2. Any output to any output, 2.5V supply | - | - | ±300 | ps |
| tLOCK | PLL Lock Time | Valid on all clock pins from VDD=2.97V | - | - | 1.0 | ms |

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS pins. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the output clocks and the load is over 1 ½ inch. The nominal impedance of the clock outputs is given on the page 4. Place the series termination resistors as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for feedback to PLL, and sees an additional 4 pF load with respect to Bank A and B clocks. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between Bank A and B clocks and CLKIN.

For minimum pin-to-pin skew, the external load at all the Bank A and B clocks must be the same.

Switching Waveforms

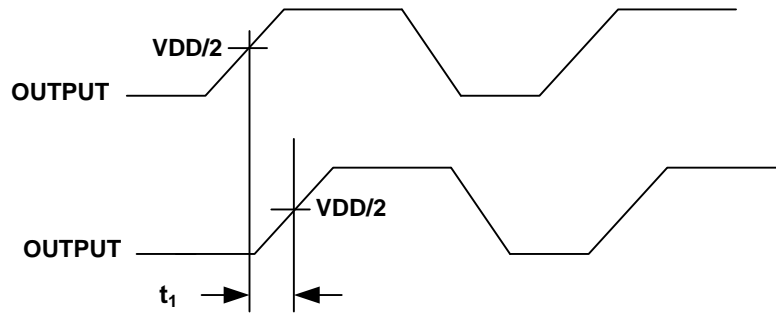


Figure 2. Output to Output Skew

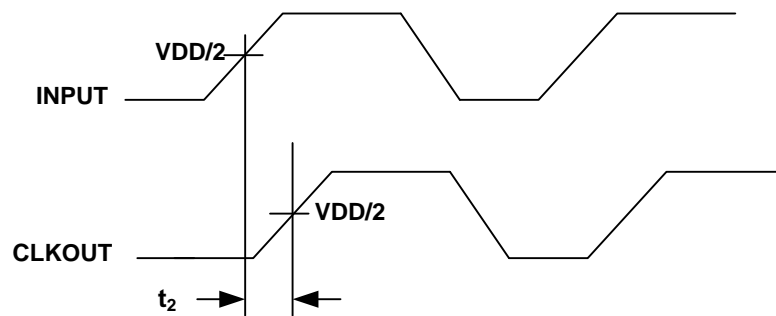


Figure 3. Input to Output Skew

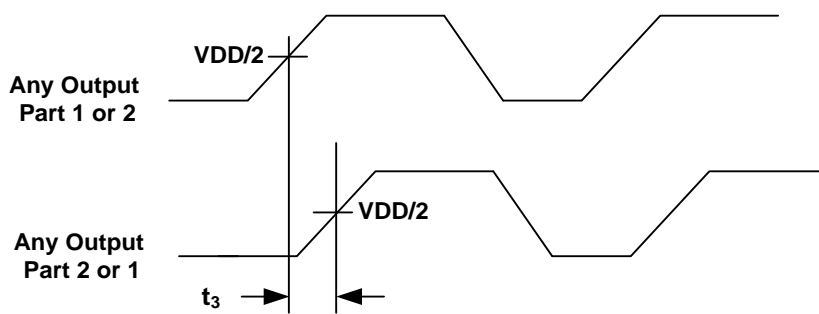
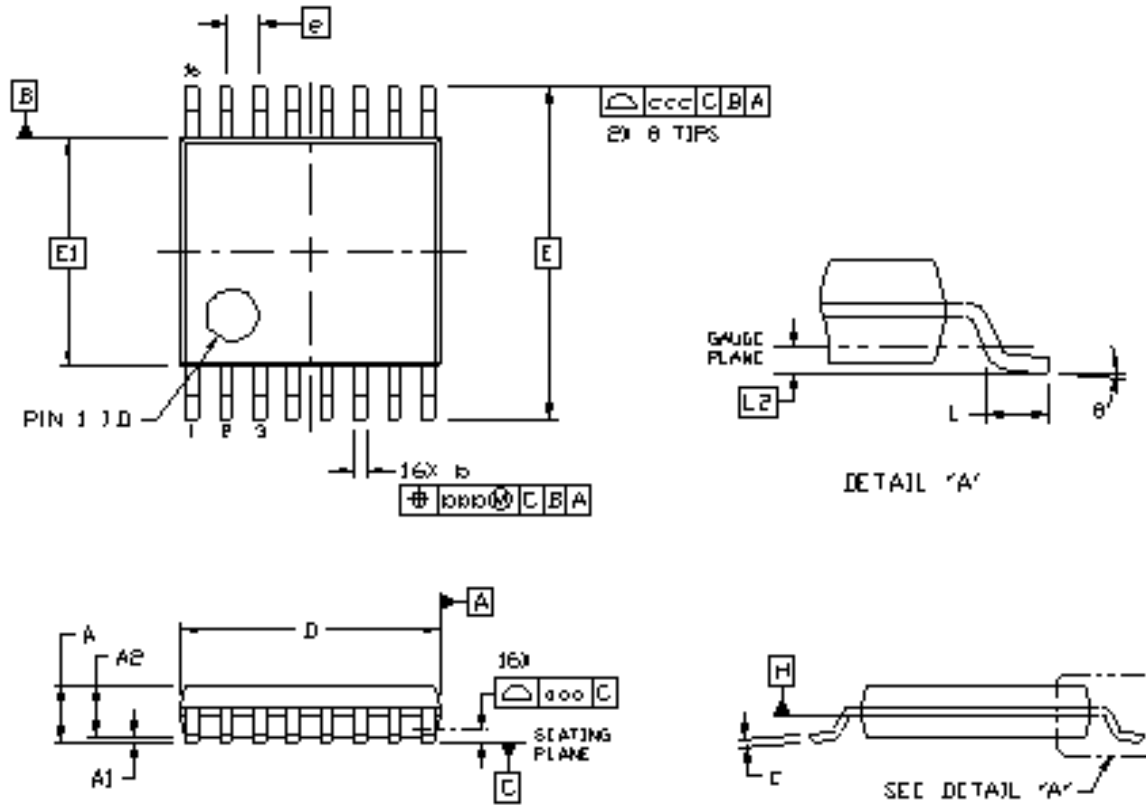


Figure 4. Part-to-Part Skew

Package Drawing and Dimensions: 16-Lead TSSOP (4.4 mm)

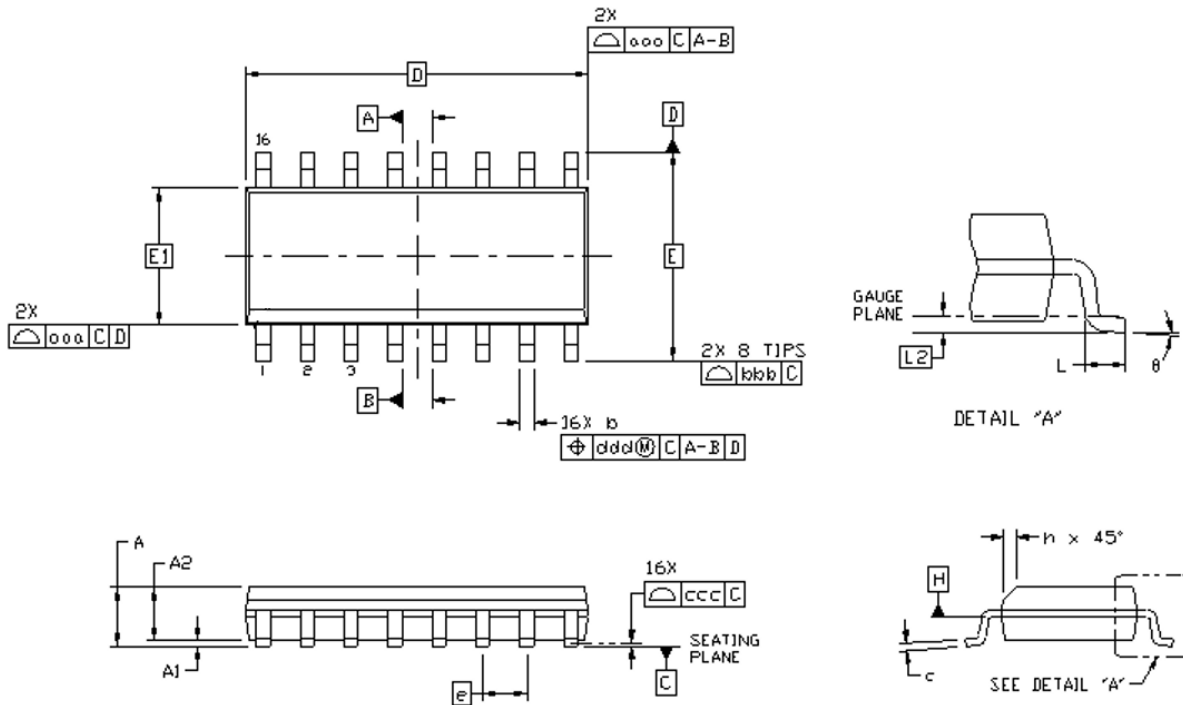


| Dimension | MIN | NOM | MAX |
|-----------|----------|------|------|
| A | -- | -- | 1.20 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | -- | 0.30 |
| c | 0.09 | -- | 0.20 |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L2 | 0.25 BSC | | |
| θ | 0° | -- | 8° |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.20 | | |

Thermal Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---------------|-------------------------|-----|-----|-----|------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | - | 80 | - | °C/W |
| | θ_{JA} | 1m/s air flow | - | 70 | - | °C/W |
| | θ_{JA} | 3m/s air flow | - | 68 | - | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | Independent of air flow | - | 36 | - | °C/W |

Package Drawing and Dimensions: 16-Lead SOIC (150 Mil)



| Dimension | MIN | MAX |
|-----------|-----------|------|
| A | -- | 1.68 |
| A1 | 0.10 | 0.25 |
| A2 | 1.30 | 1.50 |
| b | 0.35 | 0.49 |
| c | 0.19 | 0.25 |
| D | 10.10 BSC | |
| E | 6.00 BSC | |
| E1 | 3.90 BSC | |
| e | 1.27 BSC | |
| L | 0.56 | 0.82 |
| L2 | 0.25 BSC | |
| h | 0.30 REF | |
| θ | 0° | 8° |
| aaa | 0.10 | |
| bbb | 0.20 | |
| ccc | 0.10 | |
| ddd | 0.25 | |

Thermal Characteristics

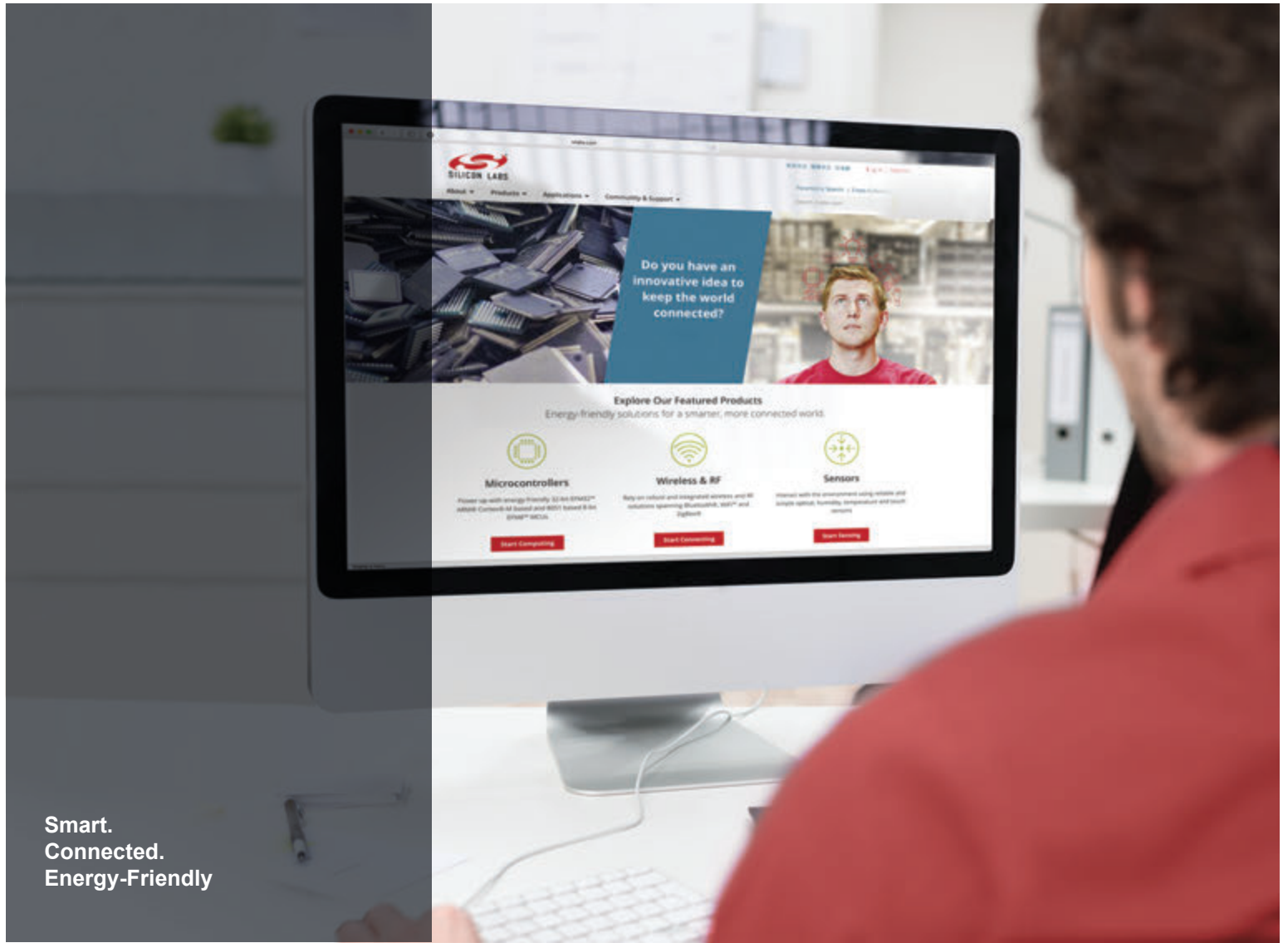
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---------------|-------------------------|-----|-----|-----|------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | - | 120 | - | °C/W |
| | θ_{JA} | 1m/s air flow | - | 115 | - | °C/W |
| | θ_{JA} | 3m/s air flow | - | 105 | - | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | Independent of air flow | - | 60 | - | °C/W |

Ordering Information ^[3]

| Ordering Number | Marking | Shipping Package | Package | Temperature |
|-----------------|---------------|------------------|--------------|-------------|
| SL23EP08SC-1 | SL23EP08SC-1 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-1T | SL23EP08SC-1 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-1 | SL23EP08SI-1 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-1T | SL23EP08SI-1 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-1H | SL23EP08SC-1H | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-1HT | SL23EP08SC-1H | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-1H | SL23EP08SI-1H | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-1HT | SL23EP08SI-1H | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08ZC-1H | SL23EP08ZC-1H | Tube | 16-pin TSSOP | 0 to 70°C |
| SL23EP08ZC-1HT | SL23EP08ZC-1H | Tape and Reel | 16-pin TSSOP | 0 to 70°C |
| SL23EP08ZI-1H | SL23EP08ZI-1H | Tube | 16-pin TSSOP | -40 to 85°C |
| SL23EP08ZI-1HT | SL23EP08ZI-1H | Tape and Reel | 16-pin TSSOP | -40 to 85°C |
| SL23EP08SC-2 | SL23EP08SC-2 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-2T | SL23EP08SC-2 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-2 | SL23EP08SI-2 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-2T | SL23EP08SI-2 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-3 | SL23EP08SC-3 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-3T | SL23EP08SC-3 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-3 | SL23EP08SI-3 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-3T | SL23EP08SI-3 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-4 | SL23EP08SC-4 | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-4T | SL23EP08SC-4 | Tape and Reel | 16-pin SOIC | 0 to 70°C |
| SL23EP08SI-4 | SL23EP08SI-4 | Tube | 16-pin SOIC | -40 to 85°C |
| SL23EP08SI-4T | SL23EP08SI-4 | Tape and Reel | 16-pin SOIC | -40 to 85°C |
| SL23EP08SC-5H | SL23EP08SC-5H | Tube | 16-pin SOIC | 0 to 70°C |
| SL23EP08SC-5HT | SL23EP08SC-5H | Tape and Reel | 16-pin SOIC | 0 to 70°C |

Notes:

- The SL23EP08 products are RoHS compliant.



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